DS33Z41DK
Ethernet Transport Design Kit

www.maxim-ic.com

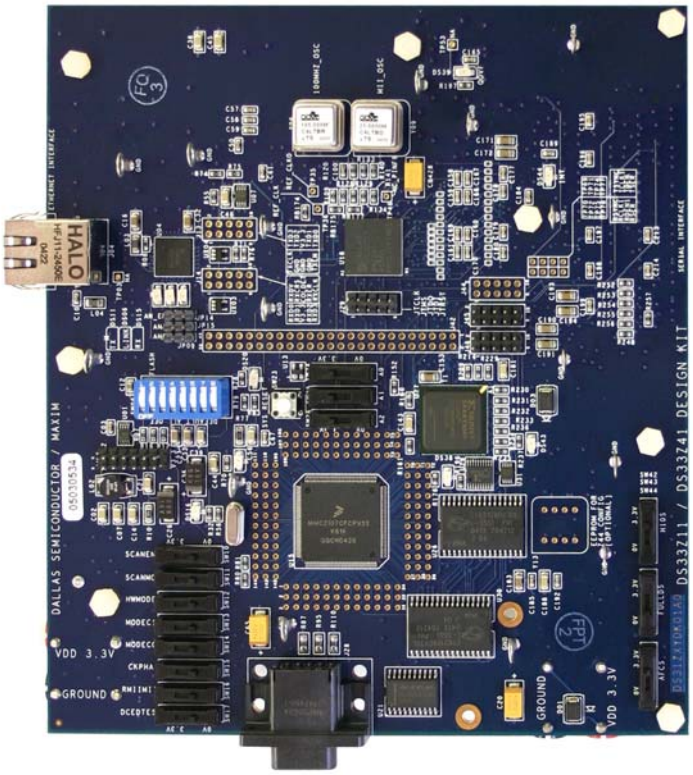
GENERAL DESCRIPTION

The DS33Z41 design kit is an easy-to-use evaluation board for the DS33Z41 Ethernet transport-over-serial link device. The DS33Z41DK is intended to be used with a resource card for the serial link. The serial link resource cards are complete with transceivers, transformers, and network connections. Dallas' ChipView software is provided with the design kit, giving point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal, queue overflow, Ethernet link, Tx/Rx, and interrupt status.

Windows is a registered trademark of Microsoft Corp.

ORDERING INFORMATION

PART	DESCRIPTION
DS33Z41DK	DS33Z41 demo card, T1/E1 transceiver resource card included



FEATURES

- Demonstrates Key Functions of DS33Z41 Ethernet Transport Chipset
- Includes Resource Card for DS21458 T1/E1 quad Transceiver with Transformers, RJ48 Network Connectors, and Termination
- Provides Support for Hardware and Software Modes
- On-Board MMC2107 Processor and ChipView Software Provide Point-and-Click Access to the DS33Z41 Register Set
- All DS33Z41 Interface Pins are Easily Accessible for External Data Source/Sink
- LEDs for Loss-of-Signal, Queue Overflow, Ethernet Link, Tx/Rx, and Interrupt Status
- Easy-to-Read Silk Screen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs

DESIGN KIT CONTENTS

- DS33Z41DK Main Board
- Quad-Port Serial Card with DS21458 T1/E1
- CD_ROM
  - ChipView Software and Manual
  - DS33Z41DK Data Sheet
  - Configuration Files

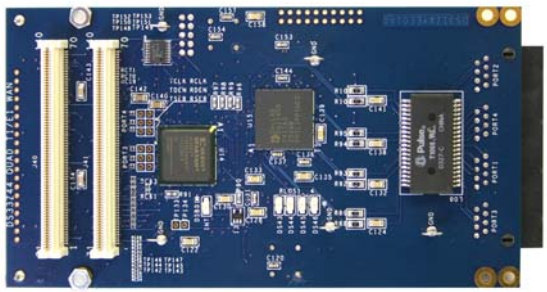


TABLE OF CONTENTS

GENERAL DESCRIPTION 1

ORDERING INFORMATION 1

DESIGN KIT CONTENTS 1

COMPONENT LIST 3

PC BOARD ERRATA 9

FILE LOCATIONS 9

BASIC OPERATION 10

POWERING UP THE DESIGN KIT 10
General 10
BASIC DS33Z41 INITIALIZATION (USED FOR ALL QUICK SETUPS) 10
Quick Setup #1 (Device Driver + DS21458 T1E1) 11
Quick Setup #2 (DS21458 T1E1, register based) 11
Configuration Note, using a single system 11
Configuration Note, a mixing device driver and register based modes 11

CONFIGURATION SWITCHES AND JUMPERS 12

ADDRESS MAP (ALL CARDS) 13

QUAD T1E1 RESOURCE CARD FPGA REGISTER MAP 14
ID REGISTERS 14
CONTROL REGISTERS 15

DS33Z41 INFORMATION 16

DS33Z41DK INFORMATION 16

TECHNICAL SUPPORT 16

SCHEMATICS 17

LIST OF FIGURES

Figure 1. System Floorplan 8
Figure 2. DS21458 Resource Card Floorplan 8
Figure 3. Schematic Hierarchy and Floorplan 17

COMPONENT LIST

Table 1 shows the component list for the DS33Z44 and DS33Z11/DS33Z41 design kits and resource cards. This BOM contains the part listing for five boards. These boards are the DS33Z41DK, DS33Z44DK, DS21458RC, DS3174RC, and DS2155-DS21348-DS3170RC. Each reference designator is only used once. For example, U18 only appears on the DS33Z41DK and is not used on any of the other boards. See Table 2.

Table 1. Component List (Decoupling Caps Not Shown)

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
U18	1	ELITE 10/100 ETHERNET TRANSPORT OVER SERIAL LINK 14X14 CSBGA 169 PIN	Dallas Semiconductor	DS33Z41
U20	1	3.3V T1.E1.J1 QUAD TRANSCEIVER 0-70C 256P BGA	Dallas Semiconductor	DS21458
U22	1	QUAD 10/100 ETHERNET EXTENSION TO WAN 17X17 PBGA 256 PIN	Dallas Semiconductor	DS33Z44
U23	1	DS3/E3 SCT, 11X11 CSBGA, 100 PIN	Dallas Semiconductor	DS3170
U24	1	T1/E1/J1 XCVR 100P QFP 0-70C	Dallas Semiconductor	DS2156L
U25	1	3.3V LIU	Dallas Semiconductor	DS21348
UB08	1	QUAD TRIPLE DUAL SINGLE ATM PACKET PHYS FOR DS3 E3 STS1 0-70C 400P BGA	Dallas Semiconductor	DS3184
U01, U09	2	SOIC 8PIN STEP-UP DC-DC CONVERTER 0.5A LIMIT	Maxim	MAX1675EUA
U07, U11	2	8-Pin µMAX/SOIC 1.8V or Adj	Maxim	MAX1792EUA18
U13, UB01	2	MICROPROCESSOR VOLTAGE MONITOR, 2.93V RESET, 4PIN SOT143	Maxim	MAX811SEUS-T
U21, UB07	2	Dual RS-232 transceivers with 3.3V/5V internal capacitors	MAXIM	NA
U31, UB06, UB11	3	8-Pin µMAX/SOIC 2.5V or Adj	Maxim	MAX1792EUA25
C11, C13, C16, C25, C27, C31–C35, C37, C41, C47, CB10, CB63, CB114, CB128, CB164, CB496	19	1206 CERAM 10uF 10V 20%	Panasonic	ECJ-3YB1A106M
CB390, CB391, CB395, CB396	4	1206 CERAM 0.1uF 25V 10%	Panasonic	ECJ-3VB1E104K
D01–D03, D05, DB03–DB05	7	SCHOTTKY DIODE, 1 AMP 40 VOLT	International Rectifier	10BQ040
DS01, DS07, DS10–DS12, DS17, DS20	7	LED, AMBER, SMD	Panasonic	LN1451C
DS02, DS03, DS09, DS14, DS15	5	L_LED, GREEN, SMD	Panasonic	LN1351C
DS04–DS06, DS08, DS13, DS16, DS18, DS27, DS28, DS35, DS37, DS38, DS40	13	LED, RED, SMD	Panasonic	LN1251C
DS19, DS43	2	LED, GREEN, SMD	Panasonic	LN1351C
DS21–DS26, DS30, DS32–DS34, DS36, DS39, DS41, DS42, DS44–DS48	19	L_LED, RED, SMD	Panasonic	LN1251C
GND_TP01–GND_TP07, GND_TP09—GND_TP44, GND_TP46–GND_TP68, GND_TPB01–GND_TPB10	76	STANDARD GROUND CLIP	KEYSTONE	4954
H1–H8, H17–H19	8	KIT, 4-40 HARDWARE, .50 NYLON STANDOFF AND NYLON HEX-NUT	NA	Lab Stock

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
H9–H16	16	KIT, 4-40 HARDWARE, 1.12 NYLON STANDOFF AND NYLON HEX-NUT (1.12 STANDOFF PN = 4807K-ND)	NA	Lab Stock
J01–J05	5	CONNECTOR, FASTJACK SINGLE, 8 PIN	Halo Electronics	HFJ11-2450E
J06, J41	2	100 MIL 2*7 POS JUMPER	NA	Lab Stock
J07–J12	6	RECEPTACLE, SMD, 140 PIN, .8MM, 2 ROW VERTICAL	AMP	5-179010-6
J13–J22	10	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT DO NOT POPLUATE	NA	Lab Stock
J23, J29, J32, J38, J39, J43, J44, J47, JB07	9	L_TERMINAL STRIP, SHROUDED, 10 PIN, DUAL ROW, VERT	3M Electronics	2510-6002UB
J24, J30, J31, J33	4	100 MIL 2 POS JUMPER	NA	Lab Stock
J25, J26, J45, J46	4	TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	NA	Lab Stock
J27, J42	2	CONN 50 PIN, 2 ROW, POSTS VERT, MOTHERBOARD FOOTPRINT	SAMTEC	TSW-125-07-T-D
J28, J36	2	L_CONN, DB9 RA, LONG CASE	AMP	747459-1
J48, J54, JB01	3	SOCKET, BANANA PLUG, HORIZONTAL, BLACK	Mouser Electronics	164-6218
J49–J52	4	CONNECTOR BNC 75 OHM VERTICAL 5PIN	Cambridge	CP-BNCPC-004
J53, JB02, JB08	3	SOCKET, BANANA PLUG, HORIZONTAL, RED	Mouser Electronics	164-6219
J55, JB11	2	L_RJ48 8 PIN SINGLE PORT CONNECTOR	MOLEX	15-43-8588
J56–J59, J61, J63	6	CONNECTOR BNC 75 OHM RA 5PIN	Trompetor	UCBJR220
J60, J62, J64, J65	4	CONNECTOR BNC RA 5PIN	Trompetor	UCBJR220
JB05, JB06, JB09, JB10, JB13, JB14	6	PLUG, SMD, 140 PIN, .8MM, 2 ROW VERTICAL	AMP	179031-6
JB12	1	RA RJ45 8PIN 4PORT JACK	MOL	43223-8140
JP01–JP19	19	100 MIL 3 POS JUMPER	NA	NA
L01, L03–L08, LB01, LB02	9	FERRITE 3A 100 OHM AT 100 MHZ 1206 SMD	Steward	HI1206N101R-00
L02, L09	2	INDUCTOR 22.0uH 2PIN SMT 20%	Coiltronics	UP1B-220
L10	1	XFMR 1-2CT XMIT, 1-1CT RCV, 40P WIDE SOIC	Pulse	T1068
R01, R02, RB10, RB11, RB18, RB19, RB22, RB23, RB26, RB27	10	RES 0603 54.9 Ohm 1/16W 1%	Panasonic	ERJ-3EKF54R9V
R03, R04, RB12, RB13, RB20, RB21, RB24, RB25, RB28, RB29	10	RES 0603 49.9 Ohm 1/16W 1%	Panasonic	ERJ-3EKF49R9V
R05, R06, R08, R09, R11	5	RES 0603 10.0K Ohm 1/16W 1% - Must be 1% tolerance	Panasonic	ERJ-3EKF1002V
R07, R12, R16, R79, R160, R244, R248, R250, R251, R254, R255, RB126, RB143, RB147, RB150, RB157	16	RES 0603 1.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ102V
R10, R107	2	RES 1206 5.6 Ohm 1/8W 5%	Panasonic	ERJ-8GEYJ5R6V
R132, R137, R142, R144, R156, RB194, RB208, RB227	8	L_RES 0603 0 Ohm 1/16W 1%	AVX	CJ10-000F

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R13–R15, R18–R20, R22, R23, R29, R30, RB01, RB03, RB07, RB09, RB15–RB17, RB30–RB32, RB34–RB38, RB41, RB44, RB47, RB48, RB50–RB52, B55, RB60, RB62, RB72, RB73, RB75, RB80, RB82	40	RES 0603 5.1K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ512V
R17, R21, R25–R28, R31, R55, R57–R59, R71, R74–R76, R83, R96–R102, R105, R106, R109, R111, R112, R115–R117, R120, R122–R126, R128, R133, R134, R140, R141, RB61, RB96, RB97, RB99, RB100, RB102–RB110, RB112, RB114–RB119, RB121, RB123–RB125, RB127, RB128, RB130, RB131, RB133, RB135–RB138, RB145, RB148, RB149, RB160, RB161, RB164, RB165, RB167–RB171, RB173–RB181, RB184, RB187, RB311, RB320, RB335, RB339, RB359	104	RES 0603 30 Ohm 1/16W	Panasonic	ERJ-3GEYJ300V
R171, R172, R174, R175, R190, R191, R240, R241	8	L_RES 0805 0.0 Ohm 1/10W 5%	Panasonic	ERJ-6GEY0R00V
R198–R200, R210–R213, RB306, RB325, RB326	10	RES 0603 332 Ohm 1/16W 1%	Panasonic	ERJ-3EKF3320V
R201–R208, RB321–RB324, RB327–RB330	16	RES 1206 0 Ohm 1/8W 5%	Panasonic	ERJ-8GEYJ0R00V
R239, RB349	2	RES 0805 51.1 Ohm 1/10W 1%	Panasonic	ERJ-6ENF51R1V
R24, R114, R197, RB14, RB33, RB40, RB42, RB43, RB49, RB53, RB54, RB57–RB59, RB71, RB77, RB78, RB152–RB156, RB221, RB234, RB251, RB284, RB304, RB331, RB332, RB342, RB344, RB350, RB354, RB360	34	L_RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
R242, R243, RB144, RB166, RB355–RB358, RB368–RB371	12	RES 0603 51 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ510V
R32, R70, R78, R161, R176, R194, R195, R237, R238, RB129, RB134, RB146, RB193	13	RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
R33–R54, R60–R69, R72, R73, R131, R136, R143, R147, R150, R154, R158, R163, R166, R169, R173, R178–R189, R215–R228, RB89–RB95, RB101, RB188–RB191, RB196–RB199, RB202–RB205, RB210–RB213, RB216–RB219, RB223–RB226, RB230–RB233, RB239–RB242, RB244–RB249, RB252–RB260, RB265–RB268, RB270-RB282, RB289–RB297	152	RES 0402 30 Ohm 1/16W 5%	Panasonic	ERJ-2GEJ300X
R56, R90	2	RES 0603 1.0M Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ105V
R77, RB159	2	L_RES 1206 0 Ohm 1/8W 5%	Panasonic	ERJ-8GEYJ0R00V
R80, R81, R84, R87, R89, R91–R93, R95, R108, R110, R118, R127, R152, R153, R196, R209, R214, R229–R236, RB200, RB237, RB238, RB263, RB264, RB286, RB287, RB300, RB301, RB333, RB364	37	RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R85, R88, R94, R104, R113, RB02, RB04–RB06, RB08, RB39, RB45, RB46, RB56, RB63–RB70, RB76, RB83, RB98, RB183, RB185, RB192, RB209, RB228, RB302, RB303, RB305, RB338, RB340, RB341, RB346–RB348, RB351–RB353, RB361–RB363, RB365–RB367	48	RES 0603 2.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ202V
R86, R103, R119, R121, R129, R130, R135, R138, R139, R145, R146, R149, R151, R157, R162, R164, R167, R168, R170, R177, R192, R193, R245-R247, R249, R252, R253, R256, R257, RB74, RB79, RB132, RB139-RB141, RB151, RB162, RB163, RB172, RB182, RB186, RB206, RB207, RB214, RB215, RB220, RB222, RB229, RB235, RB236, RB243, RB250, RB261, RB262, RB269, RB308–RB310, RB343, RB345	61	L_RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V
RB201, RB285	2	RES 0805 330 Ohm 1/10W 5%	Panasonic	ERJ-6GEYJ331V
RB283	1	RES 0603 10K Ohm 1/10W 5% - SEE SPECIAL INSTRUCTIONS	Panasonic	603_ERJ-3GEYJ103V
RB298, RB299, RB312–RB319, RB336, RB337	12	RES 0805 61.9 Ohm 1/10W 1%	Panasonic	ERJ-6ENF61R9V
RB81, RB84–RB88, RB111, RB113, RB120, RB122	10	RES 0603 DO NOT POPULATE	NA	NA
SW01–SW05, SW08–SW21, SW24–SW26, SW29–SW31, SW33–SW44	37	L_SWITCH, SP3T SLIDE, 4PIN TH	Tyco	3-1437575-3
SW06, SW22	2	L_SWITH 8POS 16PIN DIP LOW PROFILE	AMP	435668-7
SW07, SW23	2	SWITCH MOM 4PIN SINGLE POLE	Panasonic	EVQPAE04M
SW27, SW28, SW32	3	L_DIPSWITCH, 10 POS	AMP	435668-9
T01, T03	2	XFMR 16P SMT	Pulse	TX1099
T02, TB01	2	XFMR, OCTAL T3/E3, 1 TO 2, SMT 32 PIN	Pulse	T3049
TP01–TP78, TPB01, TPB02	80	TESTPOINT, 1 PLATED HOLE, DO NOT STUFF	NA	NA
U02–U06	5	IC, DsPHYTER11-SINGLE 10/100 ETHERNET TRANSCEIVER, 65 PIN LLP	National Semiconductor	DP83847ALQA56A
U08, U12, U29	3	1MBit Flash based config mem	Avnet	XCF01SV020C
U10	1	XILINX SPARTAN xc200 2.5V FPGA,256 PIN BGA	Xilinx	XC2S200-5FG256C
U14, U26, U30, UB05	4	CYPRESS SRAM, LAB STOCK	NA	NA
U15, U19	2	mmc2107 processor	Motorola	MMC2107
U16, U27	2	XILINX SPARTAN 2.5V FPGA,256 PIN BGA	Xilinx	XC2S50-5FG256C
U17, U28, U32	3	10 pin res pack, 10K ohm	NA	NA
UB02, UB03, UB04	3	100 PIN CPLD	XILINX	XC95144XL-10TQ100C
UB09, UB10	2	SYNCHRONOUS DRAM, 1MEGX32X4 BANKS, TSOP 86 PIN	Micron	MT48LC4M32B2TG-7

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
UX01–UX12, UXB02–UXB04, UXB06–UXB08	18	HIGH SPEED BUFFER	Fairchild	NC7SZ86
UXB01, UXB05	2	HIGH SPEED INVERTER	Fairchild	NC7SZ86
X01, X02	2	XTAL LOW PROFILE 8.0MHZ	ECL	EC1-8.000M
Y01, Y09	2	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 25.000 MHZ, Low Jitter required for PHY	SaRonix	NTH089AA3-25.000
Y02, Y13	2	SPI SERIAL EEPROM 16K 8 PIN DIP 2.7V NEEDS SOCKET	Atmel	AT25160A-10PI-2.7
Y03	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 2.048 MHZ	SaRonix	NTH039A3-2.0480
Y05, Y06	2	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 100.000 MHZ	SaRonix	NTH089A3-100.0000
Y07	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 44.736 MHZ	SaRonix	NTH089AA3-44.736
Y08	1	OSCILLATOR, CRYSTAL CLOCK, 5.0V - 44.736 MHZ	SaRonix	NTH089AA-44.736
YB02	1	L_OSCILLATOR, CRYSTAL CLOCK, 3.3V - 2.048 MHZ	SaRonix	NTH039A3-2.0480

Figure 1. System Floorplan

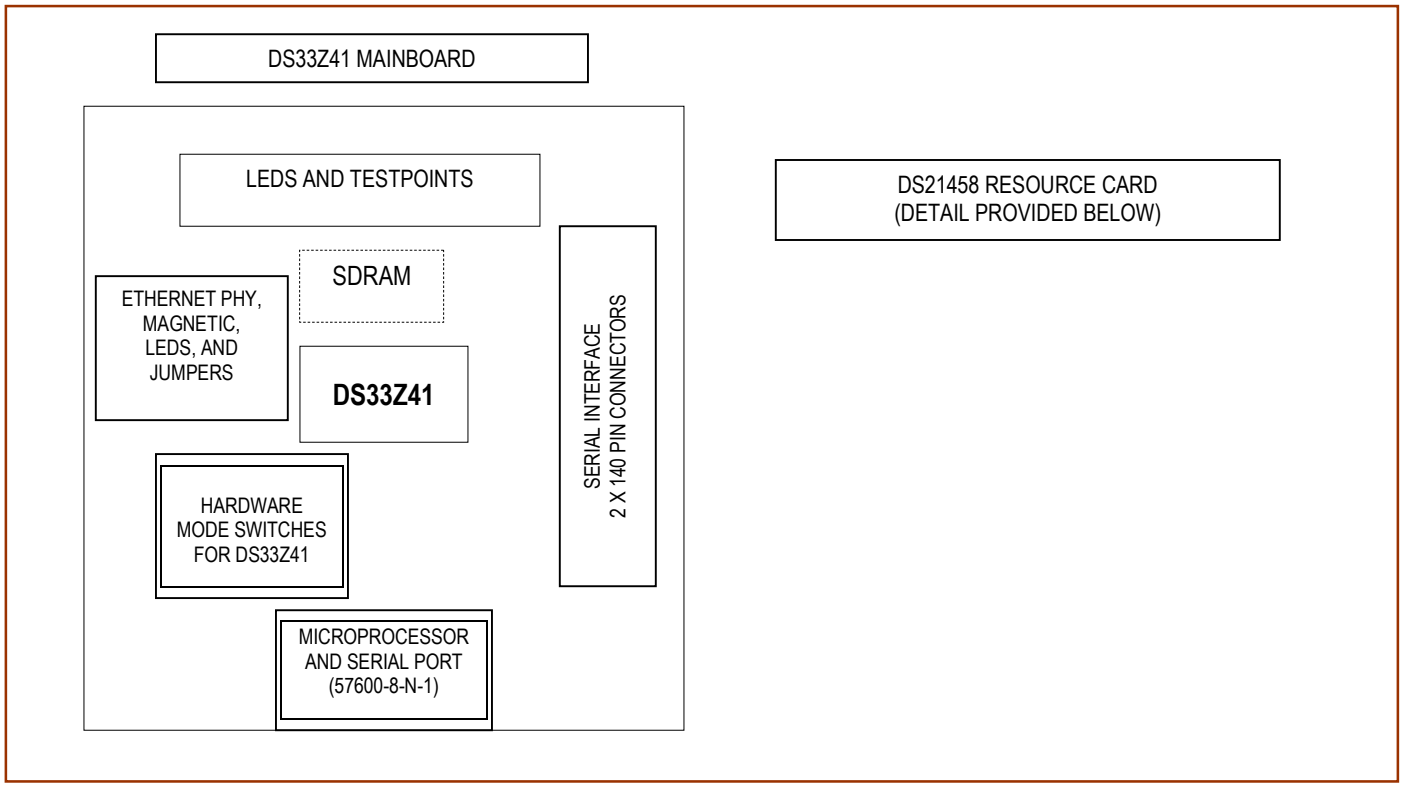
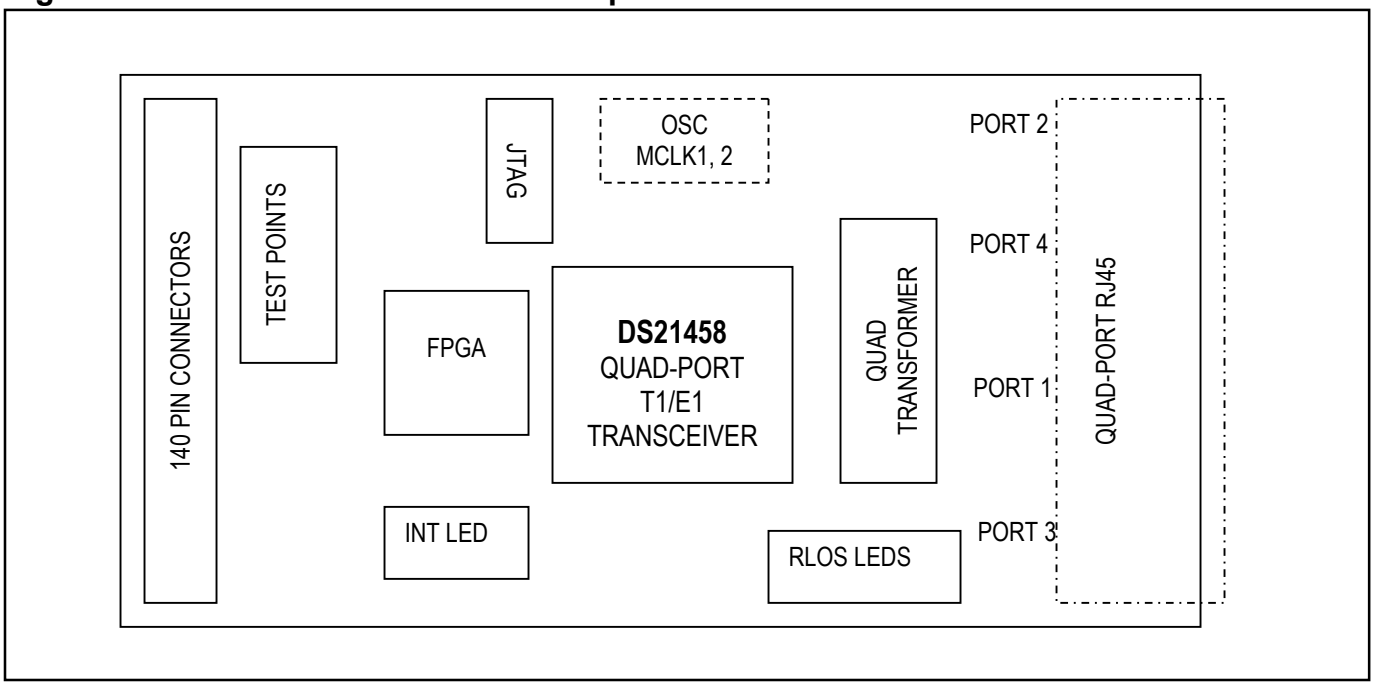


Figure 2 shows the DS21458 quad T1/E1 PC board floorplan. The current configuration is to populate oscillators for MCLK1 with a 8.192MHz oscillator. Testpoints for port 3 and port 4 are provided on the WAN card, and testpoints for ports 1 and 2 are provided on the motherboard.

Figure 2. DS21458 Resource Card Floorplan



PC BOARD ERRATA

- Silkscreen for JTAG connector signal descriptions is incorrect on the quad T1E1 card. This should be corrected with an adhesive label.

FILE LOCATIONS

This design kit relies upon several supporting files, which are provided on the CD and are available as a zip file from the Maxim website at www.maxim-ic.com/DS33Z41DK.

All locations are given relative to the top directory of the CD/zip file.

- DS33Z41 register definition files and configuration files:
    - .\cfg_demo_gui\DS33Z41_cfg_demo_gui\DS33Z41.def
    - .\DS33Z41_cfg_demo_gui\SU_LI_PORT1.def
    - .\DS33Z41_cfg_demo_gui\z41_basic.mfg

- DS21458 register definition files and configuration files:
    - .\DS33Z41_cfg_demo_gui\Qt1e1_DS21458\DS21458RC_FPGA.def
    - .\DS33Z41_cfg_demo_gui\Qt1e1_DS21458\DS21458RC.def
    - .\DS33Z41_cfg_demo_gui\Qt1e1_DS21458\T1_IBO_ LoopTime.ini
    - .\DS33Z41_cfg_demo_gui\Qt1e1_DS21458\T1_IBO_ SourceTime.ini
    - .\DS33Z41_cfg_demo_gui\Qt1e1_DS21458\E1_CRC_HDB3_IBO_ SourceTime.ini
    - .\DS33Z41_cfg_demo_gui\Qt1e1_DS21458\E1_CRC_HDB3_IBO_ LoopTime.ini

BASIC OPERATION

Powering Up the Design Kit

- Attach DS21458 resource card to main board.
- Connect PCB 3.3V and GND banana plugs to power supply. At power-up the system should draw approximately 1A.
- Set switches for software mode as described in Table 2 (short description follows).
  - Top left bank: All low, except for MODEC0, which is high.
  - Top right bank: A2, A1, A0 in mid position, SCANTRI low
  - Bottom Bank: All high (AFCS, FULLDS, H1OS)

General

- Upon power-up, the processor FPGA Status LEDs (DS43 green) will be lit. Interrupt LEDs (DS44 red) will not be lit. DS33Z11 Queue overflow LEDs (DS39 red) will not be lit. PHY LINK LED (DS06 green) should be lit if the Ethernet is connected.

Following are several basic system initializations. These initializations assume that there are two boards present (DS33Z41 and / or DS33R41). A note is provided below to assist with using a system that only contains one board.

Basic DS33Z41 Initialization (Used for All Quick Setups)

This section covers four basic methods for configuring the DS33Z41. Any one of these initializations can be used with the following Quick Setup examples:

1. Upon power-up, the on-board device driver provides a basic configuration for the DS33Z41 and attached serial cards. This enables traffic to pass from the Ethernet port to the serial port. Consult the device driver documentation for further details. Device driver behavior is dependant upon jumper settings, which are detailed in Table 2.
2. Launch ChipView.exe and select *Register View.* When prompted for a definition file, pick the file named **DS33Z41.def**. Following this load the definition file named **DS21458RC_FPGA.def**
3. Hardware Mode is not available with this DK
4. EEPROM mode is not available with this DK.
5. Ethernet Traffic generation and analysis:
   a. Using a patch cable, connect the Ethernet connector to an ordinary PC, or network test equipment. This should cause the link LED to turn on.
   b. Although ping is mentioned it is *not* recommended. The ping command goes through the computers TCPIP stack, and will sometimes will not be sent out the PCs network connector (i.e. if the PCs ARP cache is out of date). Additionally ping requires two PCs, as a PC can not ping itself (a local ping gets sent to 'localhost' instead of out the connector). With that said – ping is still a valuable test once the prototyping stage is complete.
   c. Generation and capture of arbitrary (raw) packets can be accomplished using CommView. A time-limited demo is available at the website www.tamos.com/products/commview.
   d. Ethereal is an excellent (and free) packet capture utility. Download is available at www.ethereal.com.
   e. Adding additional Ethernet ports to a PC is rather simple when a USB-to-Ethernet adapter is used. This allows for end-to-end testing using a single PC. When using two adapters the PC will have a different IP address for each adapter. Test equipment will allow selection of either adapter. Operating system based network traffic will be sent out the default adapter, usually this is the adapter that has recently had connection to a real network.

Quick Setup #1 (Device Driver + DS21458 T1E1)

- Select TCLK source for the DS21458 resource card. If this is the only DS33Z41 in the system (i.e. used in loopback) then select TCLK=MCLK. From table 2 this requires that the J45.3+J45.4 jumper is not installed. If this is the second DS33Z41 in the system select TCLK=RCLK, which requires that J45.3+J45.4 jumper is installed. Note – the TCLK source settings can be changed using the driver interface, which is described below.
- Complete the hardware configuration and one of the basic DS33Z41 configurations as described in the previous section.
- At this point any packets sent to the DS33Z41 are sent out the T1E1 ports. Incoming Ethernet packets should cause the RX LED to blink, transmitted packets cause the TX LED should also blink.
- Launch ChipView.exe, select Register View
- To interact with the device driver go to ChipView and select from the drop down menu:
  - Tools→Plugins→Load Plugins. When asked if DLLs have already registered select yes
  - Select Tools→Plugins→DS33Z41/11/41 Device Driver Demo
  - A new form called 'Zchip Configuration' appears
  - Preload basic configuration for the GUI by selecting File→Load Settings (in the 'Zchip Configuration' form). Select the file named 'basic_Config.eset'

Quick Setup #2 (DS21458 T1E1, register based)

1. Disable device drivers and callbacks – remove all jumpers from J45 header. Press the reset button, or cycle power on the board to restore the system to its power-on state.
2. Configure the DS33Z41. After the definition files load, go to the File menu and select File→Memory Config File→Load .MFG file. When prompted, select the file named **z41_basic.mfg**.
3. Set the DS2148 serial card for IBO mode. Using the menu marked 'Def File Selection' switch to the DS21458RC_FPGA def file. Set the register MO+CLK to 0x47.
4. Configure the DS21458. Go to the File menu and select File→Register INI File→Load .INI file. When prompted, select either the file named **T1_IBO_ SourceTime.ini** (TCLK=MCLK) or **T1_IBO_ LoopTime.ini** (TCLK=RCLK). Set one board to be the source of network timing (TCLK=MCLK), and one board to follow the timing source (TCLK=RCLK). The RLOS LEDs should go out when this step is complete for both boards.
5. Additional setup (for both boards):

- Switch to the DS33Z41 def file and set the following:
  - Set the GL.IMUXCN register to 0x0F (both systems)
  - Set GL.IMUXC register to 0x00 then to 0x82 (both systems)
  - Check GL.IMUXSS register. They should be 0xFF on both systems
  - Return to GL.IMUXCN and set the bits RXE and SENDE
  - The system should now be configured to pass Ethernet traffic into one system and out of the other.

Configuration Note, using a single system

The DS33Z41 is intended for use in a system with a DS33Z41 at each end. However, the system may be tested with only a single DS33Z41 system. This configuration requires that the DS21458 serial link is in loopback, either internal loopback or hardware loopback may be used. In this configuration any packets sent to the Ethernet side will be echoed back. In this configuration the setting for DS21458 TCLK=MCLK should be used (see table 2), and steps intended for the 'second' system may be ignored.

Configuration Note, a mixing device driver and register based modes

Quick setup #1 discuses device driver based operation. Quick setup #2 discusses register based operation. To some extent both modes may be used simultaneously to gain insight to device configuration. For example:

- In register view click "Read All" this causes all registers to be read, changed registers turn green.
- Switch to the device driver GUI, select one of the forms, make changes, and click "send configuration"
- Switch back to register view and click "Read All". Newly changed registers will turn green, showing which registers changed as a result of settings selected in the device driver GUI

A second type of device driver / register based configuration is to power the board with the device drivers enabled, and then remove the jumpers that enable the device drivers. This allows for a fast initial configuration.

CONFIGURATION SWITCHES AND JUMPERS

The DS33Z41DK has several configuration switches, banana plugs, oscillators, and jumpers. Table 2 provides a description of these signals, given in order of appearance on the PC board (going from left to right, top to bottom).

Table 2. Main Board PC Board Configuration

SILK SCREEN REFERENCE	FUNCTION	BASIC SETTING		DESCRIPTION
		SW MODE	HW MODE	
J25.9 + J25.10	Reserved	Not installed	—	This jumper is not for use with the DS33Z41 design kit. Pin J25.10 has been removed to prevent accidental installation
J25.7 + J25.8	Enable device driver	User decision	—	When installed the device driver will configure the DS33Z41 and the Transceiver during power-up.
J25.5 + J25.6	Enable callbacks	User decision	—	When installed the driver will respond to interrupts
J25.3 + J25.4	Select TCLK source	User decision	—	When installed the driver will configure DS21458 TCLK to be sourced from DS21458 RCLK. When not installed DS21458 scaled MCLK is used. This setting is only applied at reset. If only one board is used select TCLK = MCLK.
GROUND (banana plug)	Power supply ground	—	—	System Ground. Always connected to power supply.
VDD 3.3V (banana plug)	Power supply VDD	—	—	System VDD. Always connected to power supply.
OnCe	BDM	—	—	Debug connector for processor
DCEDTES (3pos switch)	DS33Z41 mode pin; DTE/DCE selection	LOW	LOW	Low for DTE
RMIIMII (3pos switch)	DS33Z41 mode pin	LOW	LOW	High for RMII, low for MII
CKPHA (3pos switch)	DS33Z41 mode pin	LOW	LOW	SPI EEPROM hardware mode configuration switch
MODEC0 (3pos switch)	DS33Z41 mode pin	HIGH	LOW	Software mode selected
MODEC1 (3pos switch)	DS33Z41 mode pin	LOW	LOW	Software mode selected
HWMODE (3pos switch)	DS33Z41 mode pin	LOW	LOW	Hardware/software mode (software mode selected)
SCANMO (3pos switch)	DS33Z41 mode pin	LOW	LOW	Set low for normal operation
SCANTRI (3pos switch)	DS33Z41 mode pin	LOW	LOW	Set low for normal operation
….testpoints….	DS33Z41 testpoints	—	—	Processor bus, JTAG and LAN side testpoints for Zchip
Z-RESET (button)	DS33Z41 reset	—	—	System reset
A2, A1, A0 (3pos switches)	DS33Z41/SPI pins	Mid position	Mid position	Address pin/EEPROM config switch. Set to mid position to allow connection to processor.
SDRAM CLOCK	DS33Z41 SDRAM clock	Installed	Installed	100MHz oscillator to drive SDRAM clock
MII CLOCK	PHY MII clock	Installed	Installed	25MHz oscillator to drive SDRAM clock

SILK SCREEN REFERENCE	FUNCTION	BASIC SETTING		DESCRIPTION
		SW MODE	HW MODE	
spi_cs, spi_ck, spi_miso, spi_mosi	—	—	—	SPI signals (for EEPROM memory)
….testpoints…..	DS33Z41 testpoints	—	—	DS33Z41 serial port testpoints
AFCS (1 per port)	DS33Z41 mode pin	HW mode only	HIGH	Set high to enable auto flow control.
FULLDS (1 per port)	DS33Z41 mode pin	HW mode only	HIGH	Set high to enable full duplex.
H10S (1 per port)	DS33Z41 mode pin	HW mode only	HIGH	Set high to confg for 100Mb.
GROUND/VDD (banana plug)	Power supply ground/3.3V	—	—	Redundant connection to system power. Use plugs at either top or bottom of board.
VDD 3.3V (banana plug)	Power supply VDD	—	—	Redundant connection to system power. Use plugs at either top or bottom of board.

ADDRESS MAP (ALL CARDS)

Motorola resource card address space begins at 0x81000000. All offsets given below are relative to the beginning of the daughter card address space (shown previously).

Table 3. Overview of Daughter Card Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0087	FPGA	Processor board identification
0X1000 to 0X1FFF	DS33Z41	DS33Z41. Uses CS_X1.
0X2000 to 0X2FFF	DS21458	T1E1 DS21458 resource card. Uses CS_X2.
0X4000 to 0X4010	FPGA	FPGA on DS21458 resource card. Used to facilitate IBO mode. Default configuration of FPGA is compatible with non-IBO mode functionality. The FPGA settings will require modification for use with the DS33Z41 when device drivers are disabled.

Registers in the DS33Z41 and DS21458 can be easily modified using the ChipView host-based user-interface software with the definition files previously mentioned.

Quad T1E1 RESOURCE CARD FPGA REGISTER MAP

Table 4. Quad T1E1 Processor Card FPGA Register Map

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0X4000	Rev	Read only	FPGA Rev
0X4001	delay_line1	Control	Line 1 number of frame delay
0X4002	delay_line2	Control	Line 2 number of frame delay
0X4003	delay_line3	Control	Line 3 number of frame delay
0X4004	delay_line4	Control	Line 4 number of frame delay
0X4005	MO+CLK	Control	Mode and clock ctrl
0X4006	UNUSED	Control	Unused / test
0X4007	UNUSED	Control	Unused / test

ID REGISTERS

REV: FPGA REV (Offset=0X4000)

FPGA Rev is read only, showing the current FPGA revision

CONTROL REGISTERS

Register Name: **delay_line1, delay_line2, delay_line3, delay_line4**
Register Description: **DS33Z41 frame delay**
Register Offset: **0X4001, 0X4002, 0X4003, 0X4004**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	B5	B4	B3	B2	B1	B0
Default	—	—	—	—	0	0	0	0

Bits 5 to 0: B5 to B0. Number of frame delay for a given line.

Register Name: **MO+CLK**
Register Description: **DS33ZXY Mode and Clock Settings**
Register Offset: **0X4005**

Bit #	7	6	5	4	3	2	1	0
Name	LB	MC	IR	tgapclk	rgapclk	comm_tclk	common_rclk	z41_mode
Default	0	—	—	1	1	0	0	0

Bit 7: LB
0 = Normal operation, traffic goes from the Z chip through the FPGA and to the DS21458.
1 = Loopback, Z chip rser is driven by Z chip tser. Clocks, and frame sync for Z41, are still driven by DS21458.

Bit 6: INVERT_RCLKh
0 = Do not invert RCLK.
1 = Invert RCLK.

Bit 5: MclkHiBpclkLow
0 = Use BPCLK for clock signals below.
1 = Use MCLK for clock signals below.
This signal drives the following clocks: TCLK (when bit for common_tclk is set); RCLK (when bit for common_rclk is set); TSYSCLK and RSYSCLK (when bit for Z41_mode is set).

Bit 4: TGAPCLK
0 = Drive internal TGAPCLKx signal with TCLKx.
1 = Drive internal TGAPCLKx signal with TGAPCLK pin.

Bit 3: RGAPCLK
0 = Drive internal RGAPCLKx signal with RCLKx.
1 = Drive internal RGAPCLKx signal with RGAPCLK pin.

Bit 2: Common TCLK
0 = Drive TCLKx with internal TGAPCLKx signal (see bit 4)
1 = Drive Z chip TCLKx with BPCLK

Bit 1: Common RCLK
0 = Drive RCLKx with internal RGAPCLKx signal (see bit 3).
1 = Drive Z chip RCLKx with BPCLK.

Bit 0: Z41 Mode
0 = Not in Z41 mode.
1 = In Z41 mode.

DS33Z41 INFORMATION

For more information about the DS33Z41, consult the DS33Z41 data sheet available on our website at www.maxim-ic.com/DS33Z41.

DS33Z41DK INFORMATION

For more information about the DS33Z41DK, including software downloads, consult the DS33Z41DK data sheet available on the our website at www.maxim-ic.com/DS33Z41DK.

TECHNICAL SUPPORT

For additional technical support, please e-mail your questions to telecom.support@dalsemi.com.

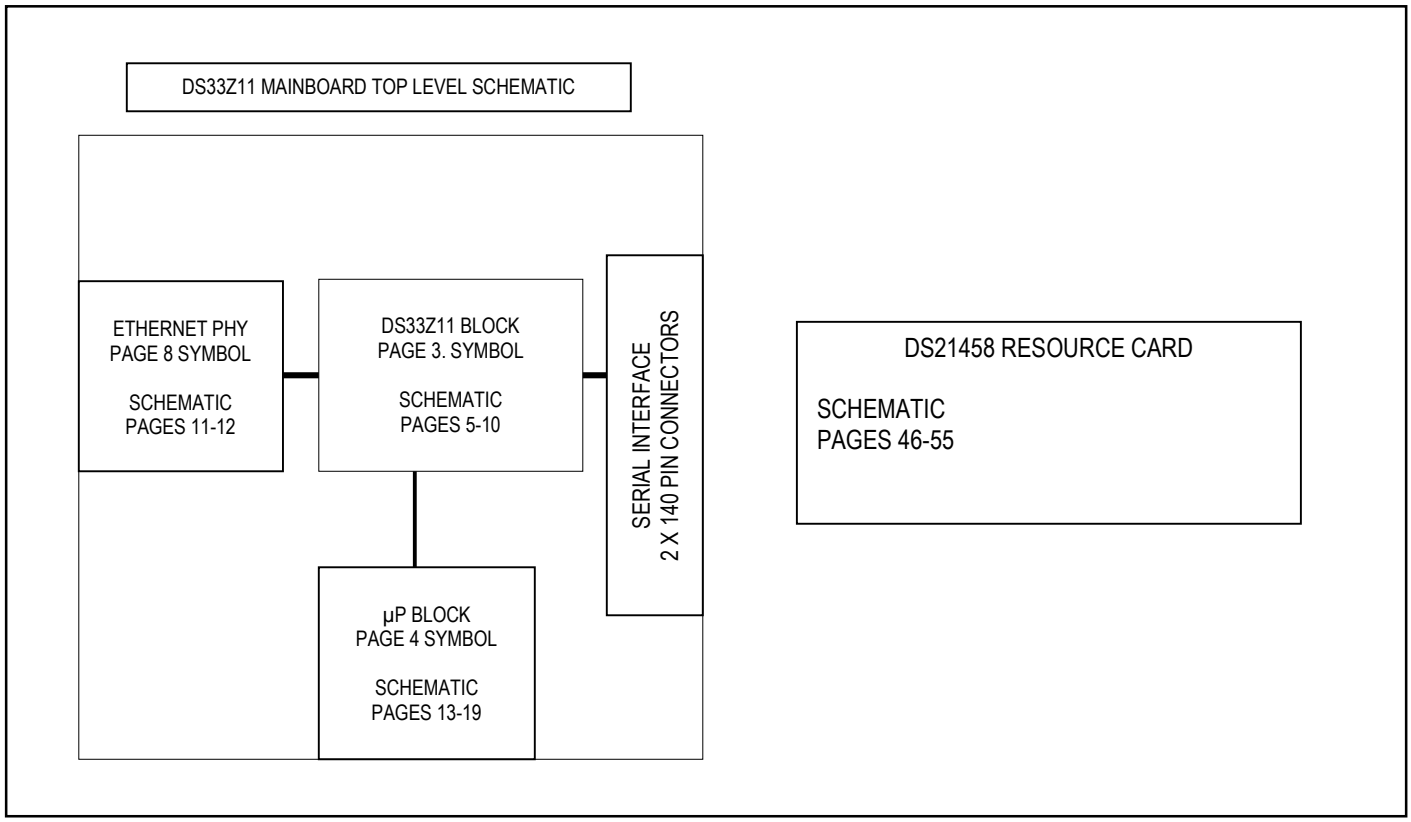
SCHEMATICS

The DS33Z41DK schematics are featured in the following pages. As this is a hierarchal schematic some explanation is in order. The main board is composed of six hierarchal blocks: the processor block, the DS33Z41 block, and four Ethernet blocks inside the DS33Z41 block, which is a nested hierarchy block. The DS21458 consists of a single hierarchy block, which connects to a 140-pin AV bus that snaps into the mainboard.

All signals inside a hierarchy block are local, with exception for V_{CC} and ground. In-port and out-port connectors are used to allow signals inside a hierarchy block to become accessible as pins on the hierarchy blocks symbol. From here, blocks are wired together as if they were ordinary components. The system diagram is shown again below, with schematic page numbers given for each functional block.

This system contained other hierarchy blocks that are not shown (primarily a single-port serial card, T3E3 serial card and the DS33Z44 mainboard). Due to this, page numbers will not be continuous and some gaps in numbering will be seen when referring to the total page count. However, page numbers inside any given hierarchy block will be continuous.

Figure 3. Schematic Hierarchy and Floorplan



DS33Z11/Z41 TOP LEVEL

V3_3

V3_3 3A5<> 3A8<> 3B5<> 3B8<> 3C5<> 3C8<> 4D8> 3D8 4D8

GND

HIERARCHICAL BLOCK

_z11andlan_dn

PAGES 5-10

5C4v 5B1v 5A1v 4C6<	A_DUT<9,,0>	ADDR<9,,0>	
5B4v 4C6<	D_DUT<7,,0>	DAT<7,,0>	
5A6v 4D3>	CS_X1	CS	INT → INT2 3C7<> 3C8<> 4D5< 5A6v
5A5v 4C5<	RD_DUT	RD	
5A5v 4C5<	WR_DUT	WR	
5A5v 4C3> 3C7<>	RESET_B	RESET_B	
6A6v 3C6<>	Z41RSYNC	Z41RSYNC	
6A6v 3C6<>	Z41TSYNC	Z41TSYNC	
		HWMODE	BTS_DUT 4B5< 5A5v
		MODEC0	BIS0_DUT 4C5< 5A5v
		MODEC1	BIS1_DUT 4B5< 5A5v

RCLKI, TCLKI, RSER, TSER, RDEN, TDEN

Z44_RCLK<1>, Z44_TCLK<1>, Z44_RSER<1>, Z44_TSER<1>, Z44_RDEN<1>, Z44_TDEN<1>

3C6<> 5C5v 3C6<> 5D5v 3C6<> 5C4v 3C8<> 5C5v

PLUG
P2 CONNECTOR (PLUG)
JB13

PLUG
P1 CONNECTOR (PLUG)
JB09

MOTHERBOARD CONNECTORS FOR WAN R.C.

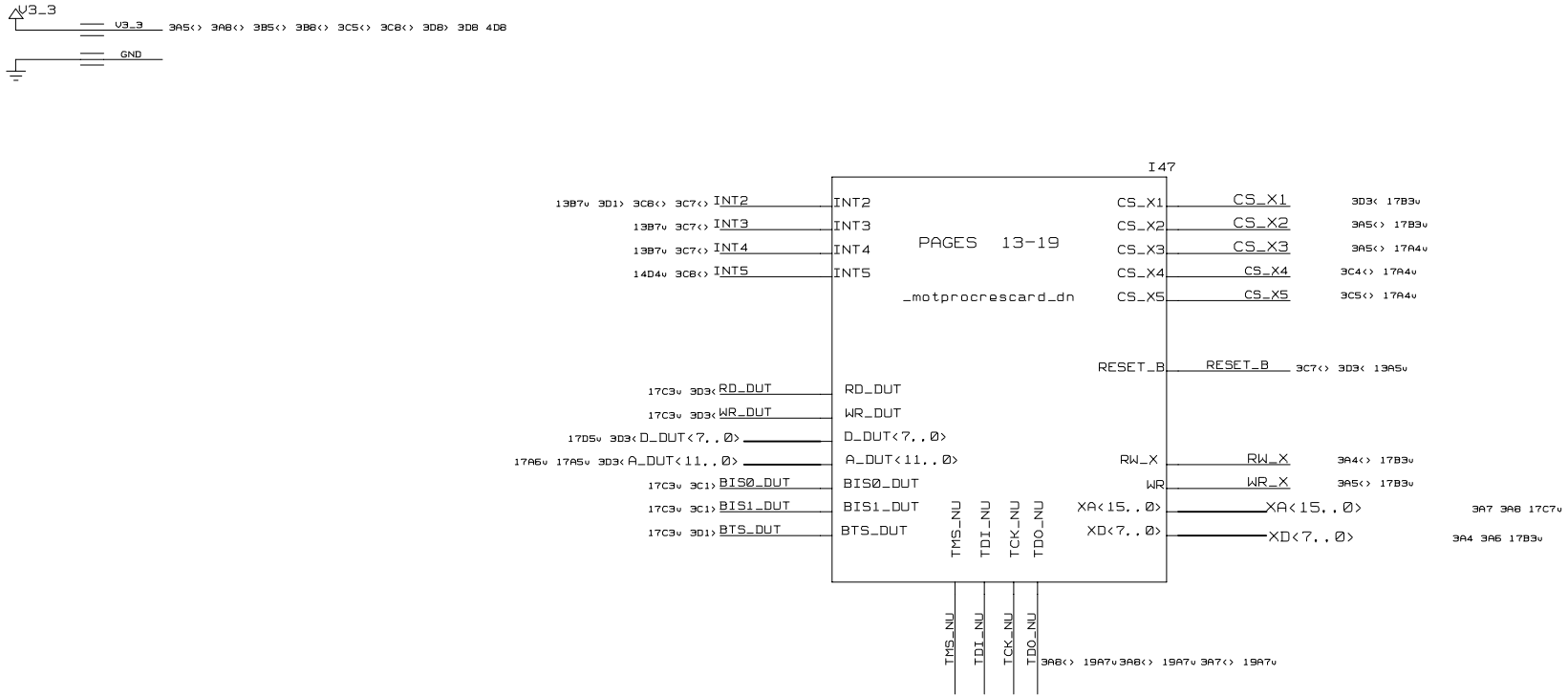
GND SIG_RETURN 3A3<> 3B7<> 3C7<>

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:1/2<BLOCK> 3/71<TOTAL>

BLOCK NAME: _z11top_dn, PARENT BLOCK: _ztopdn_\

PRINTED Tue Apr 26 14:22:51 2005

CR-4 : @_ZTOP_LIB\,_ZTOPDN_\(SCH_1):PAGE1_IS@_ZTOP_LIB\,_Z11TOP_DN\(SCH_1):PAGE2



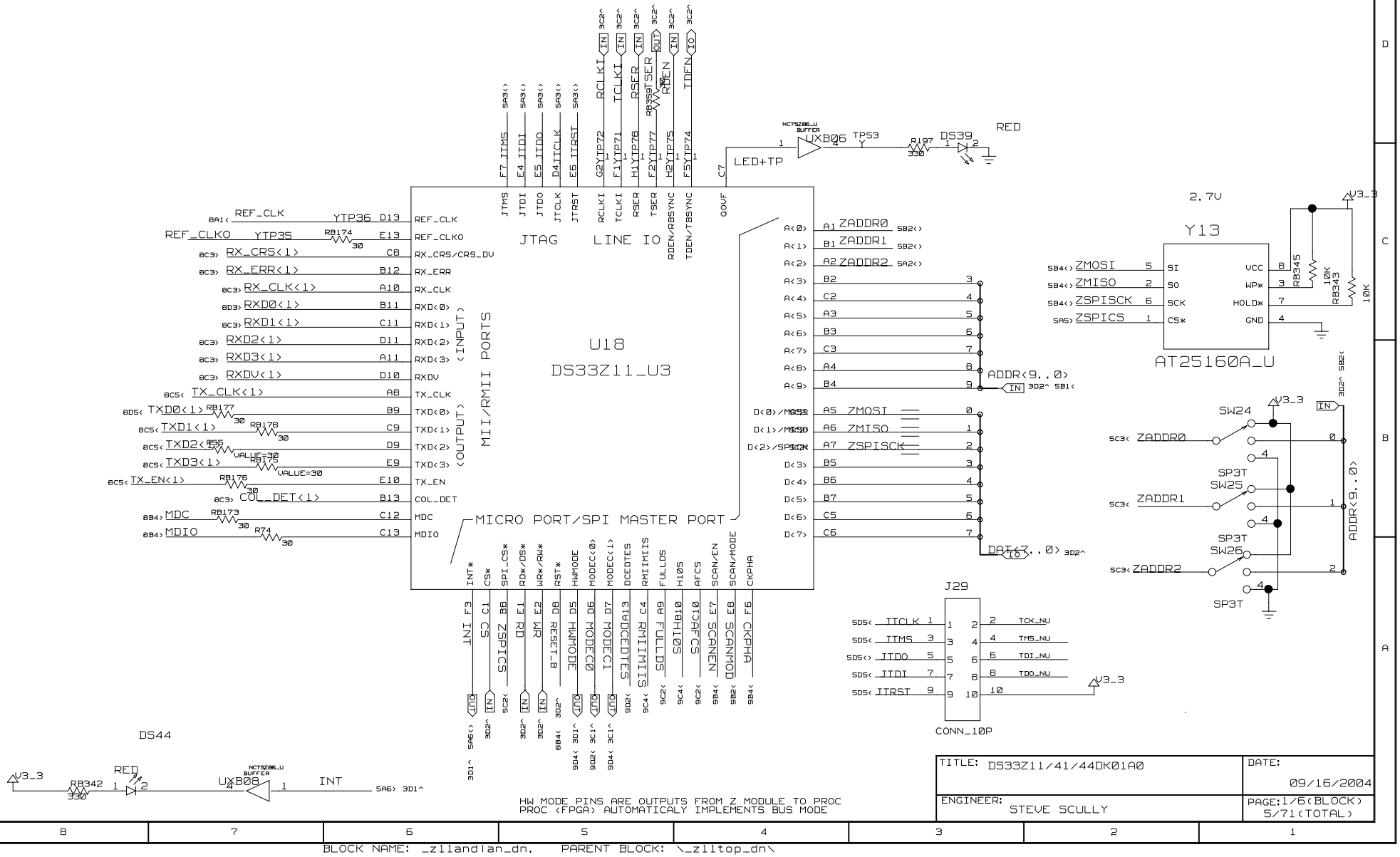
TITLE: DS33Z11/41/44DK01A0	DATE: 09/15/2004
ENGINEER: STEVE SCULLY	PAGE:2/2‹BLOCK› 4/71‹TOTAL›

BLOCK NAME: _z11top_dn, PARENT BLOCK: _ztopdn_\

JMP_3

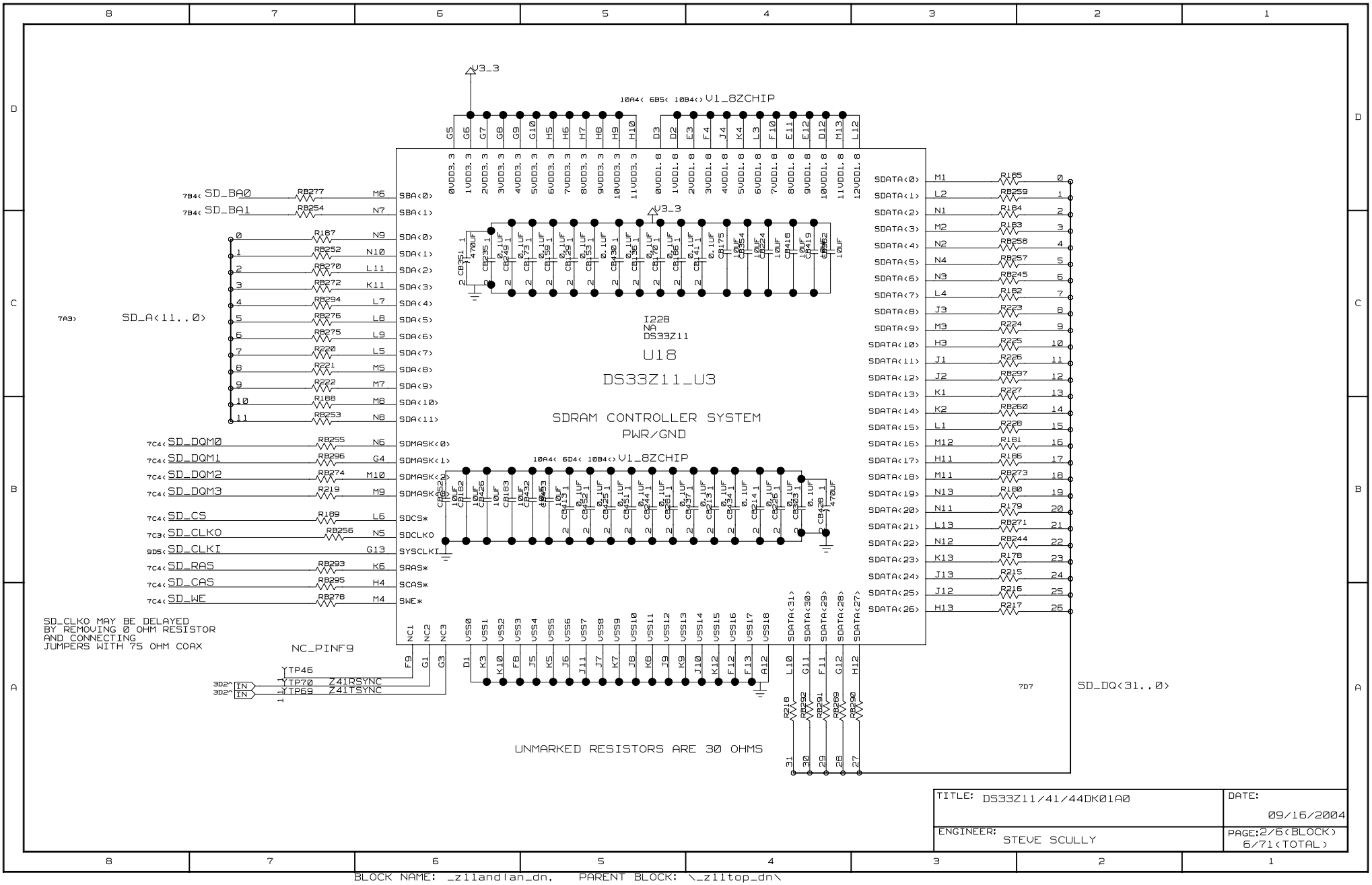
CR-5 : @_ZTOP_LIB\,_ZTOPDN_\(SCH_1):PAGE1_IS@_ZTOP_LIB\,_Z11TOP_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\,_Z11ANDLAN_DN\(SCH_1):PAGE1

DS33Z11/Z41



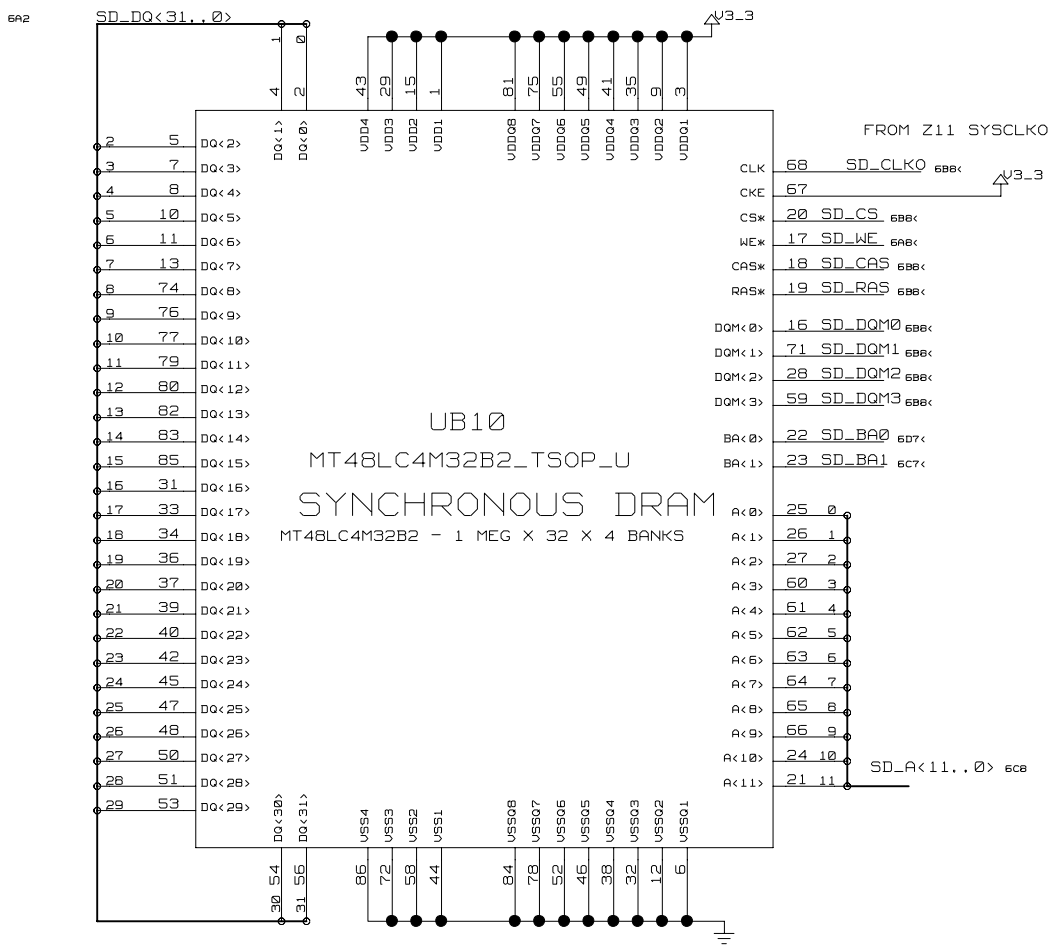
TITLE: DS33Z11/41/44DK01A0	DATE: 09/15/2004
ENGINEER: STEVE SCULLY	PAGE:1/6(BLOCK) 5/71(TOTAL)

BLOCK NAME: _z11andlan_dn, PARENT BLOCK: _z11top_dn\



TITLE: DS33Z11/41/44DK01A0	DATE: 09/15/2004
ENGINEER: STEVE SCULLY	PAGE:2/6(BLOCK) 6/71(TOTAL)

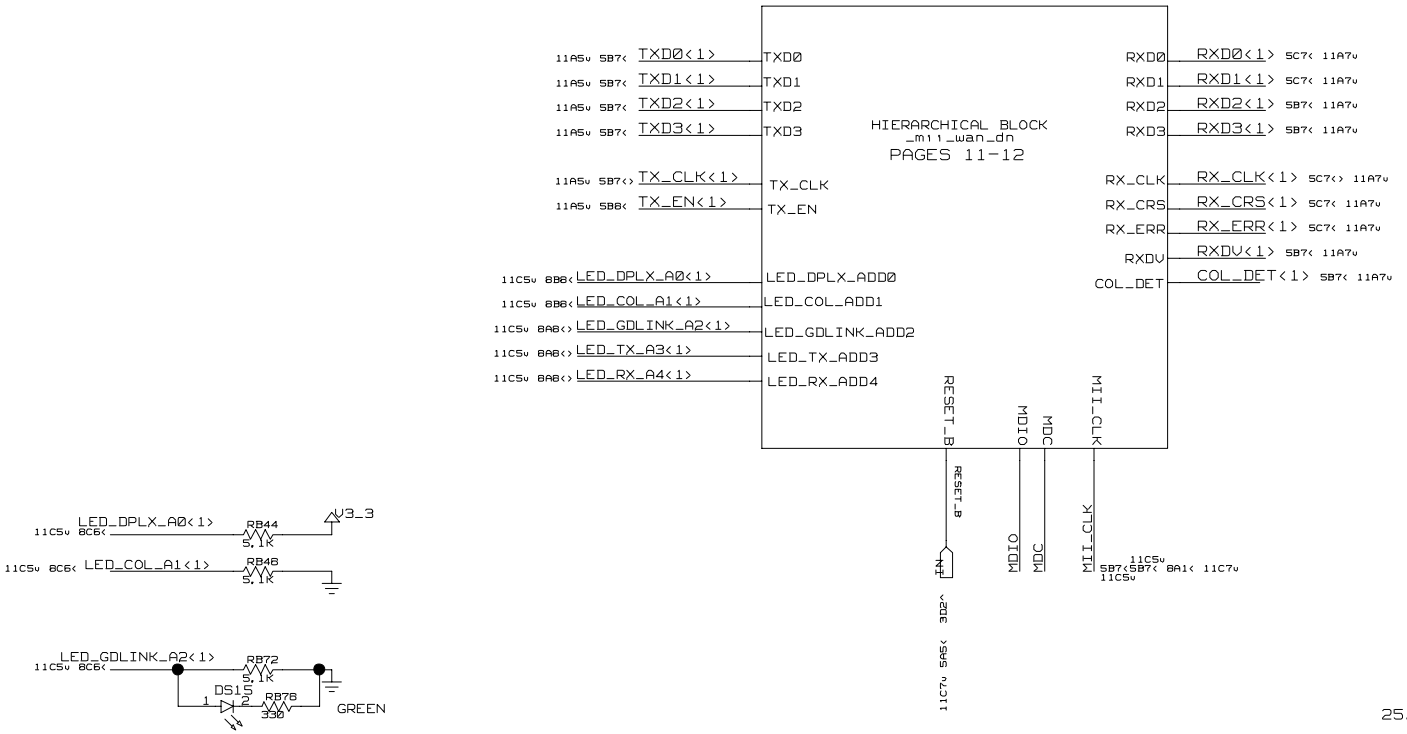
BLOCK NAME: _z11andlan_dn, PARENT BLOCK: _z11top_dn\

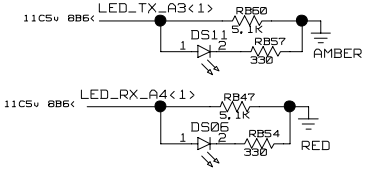


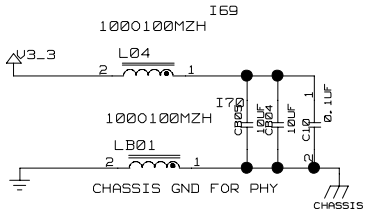
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:3/6(BLOCK) 7/71(TOTAL)

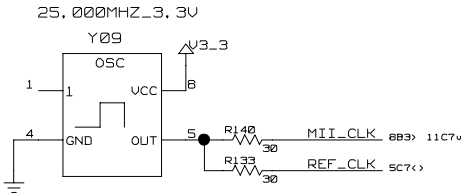
BLOCK NAME: _z11andlan_dn, PARENT BLOCK: _z11top_dn\

CR-8 : @_ZTOP_LIB\,_ZTOPDN_\(SCH_1):PAGE1_IS@_ZTOP_LIB\,_Z11TOP_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\,_Z11ANDLAN_DN\(SCH_1):PAGE4





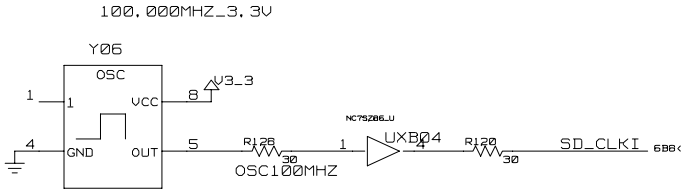


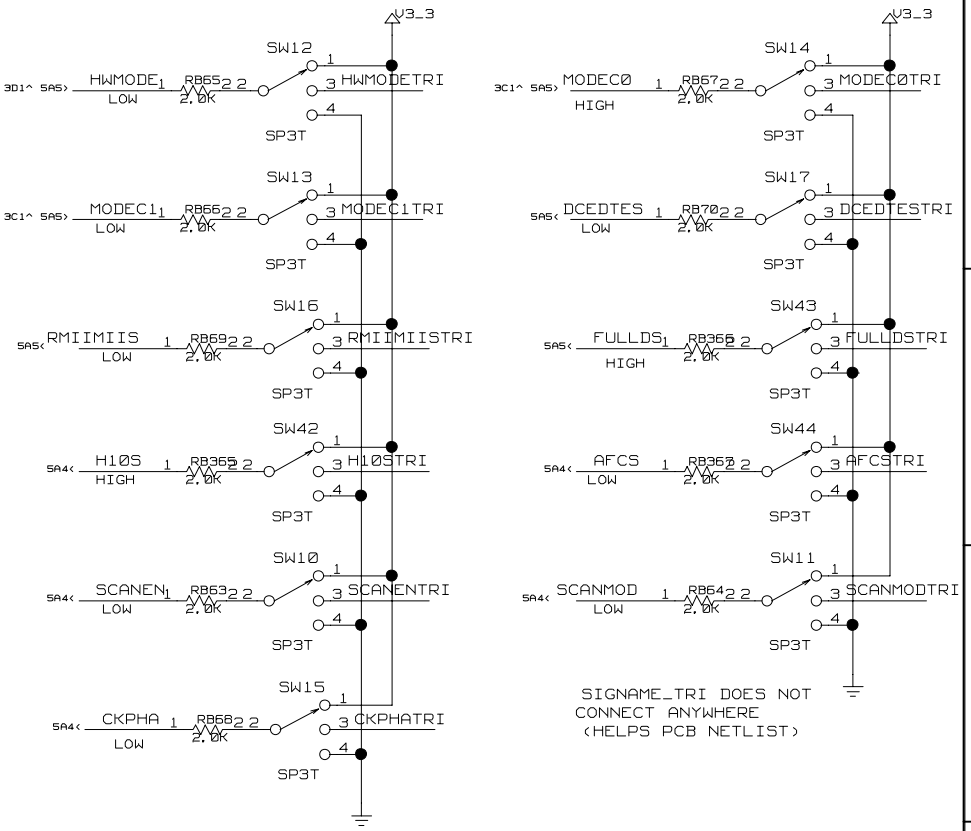


TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:4/6(BLOCK) 8/71(TOTAL)

BLOCK NAME: _z11andlan_dn. PARENT BLOCK: _z11top_dn\

CR-9 : @_ZTOP_LIB\,_ZTOPDN_\(SCH_1):PAGE1_IS@_ZTOP_LIB\,_Z11TOP_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\,_Z11ANDLAN_DN\(SCH_1):PAGE5





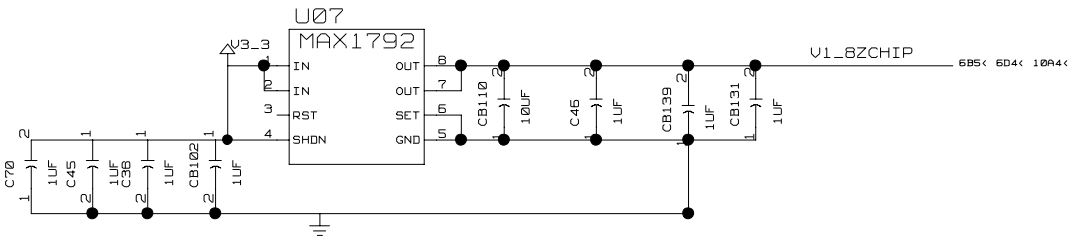
MODE (SHOWN BELOW SIGNAL) RESULTS IN:
MOTOROLA NON-MUX, MII, FULL DUPLEX, 100 MBIT, AUTO-FLOW CONTROL

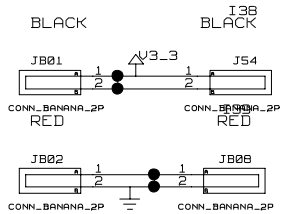
CONFIG SWITCHES FOR Z11

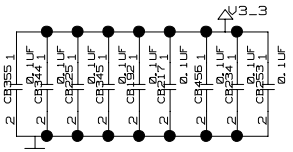
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:5/6(BLOCK) 9/71(TOTAL)

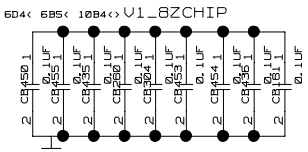
BLOCK NAME: _z11andlan_dn, PARENT BLOCK: _z11top_dn\

CR-10 : @_ZTOP_LIB\,_ZTOPDN_\(SCH_1):PAGE1_I5@_ZTOP_LIB\,_Z11TOP_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\,_Z11ANDLAN_DN\(SCH_1):PAGE6



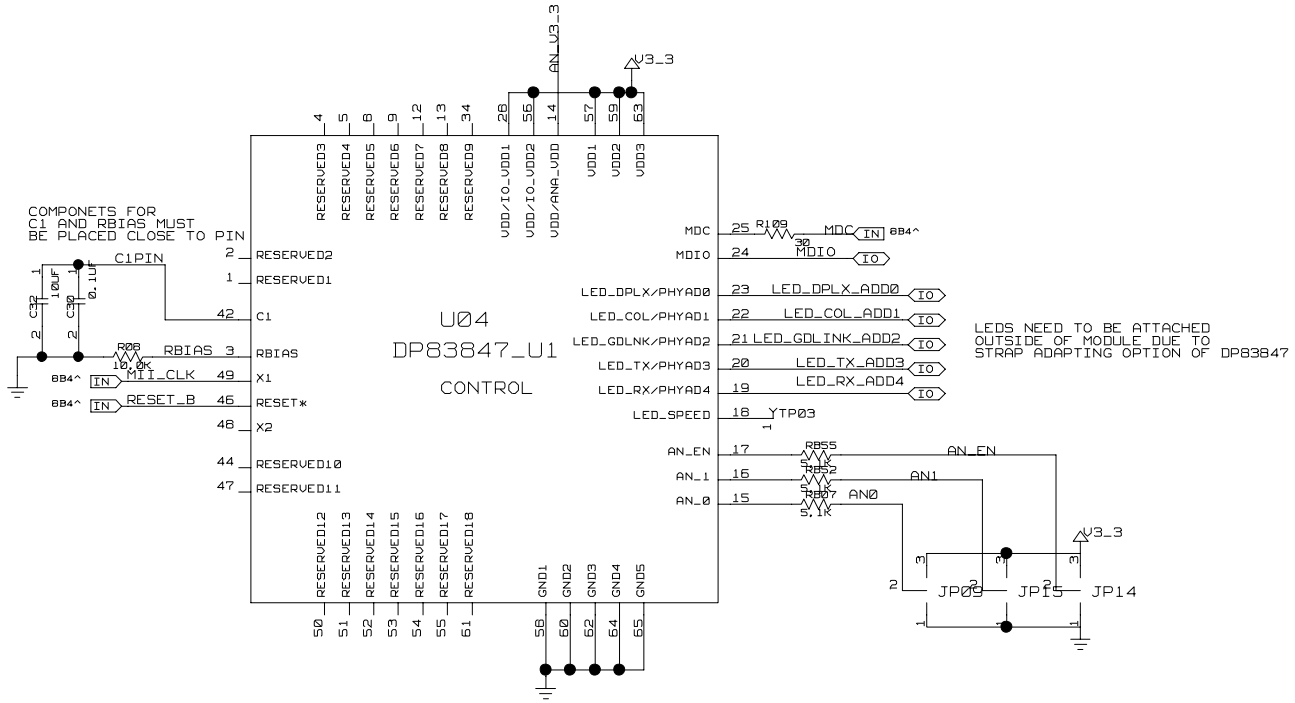


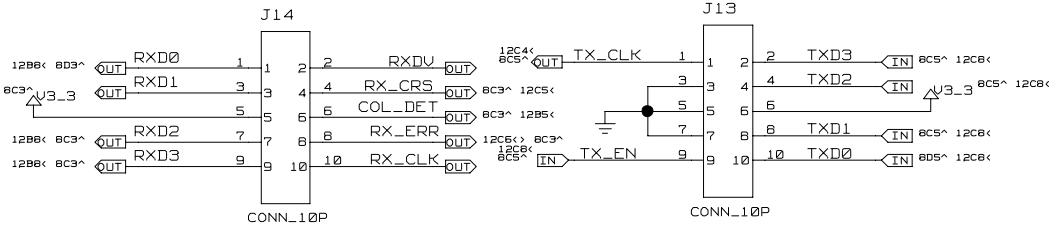


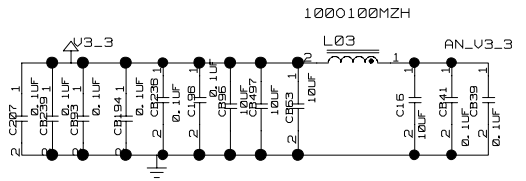


TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:6/6(BLOCK) 10/71(TOTAL)

BLOCK NAME: _z11andlan_dn. PARENT BLOCK: _z11top_dn\



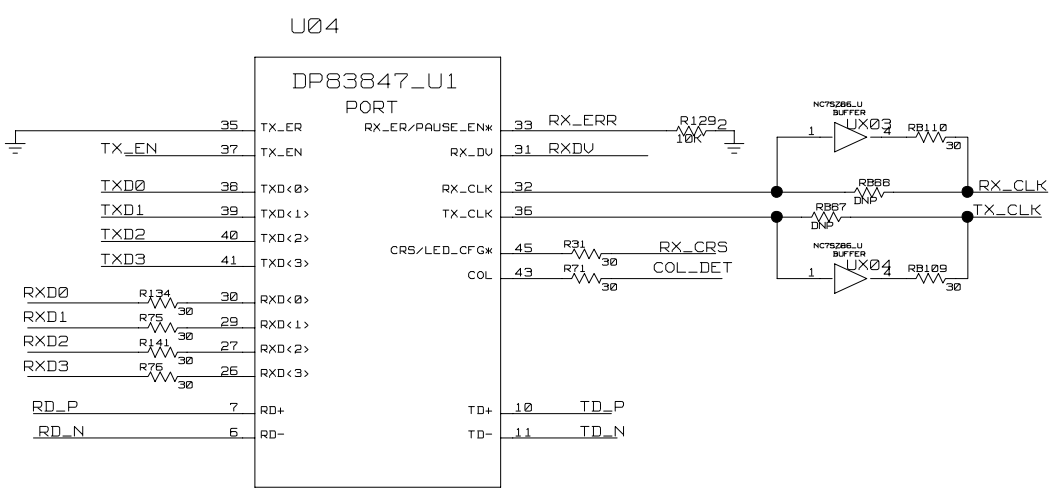


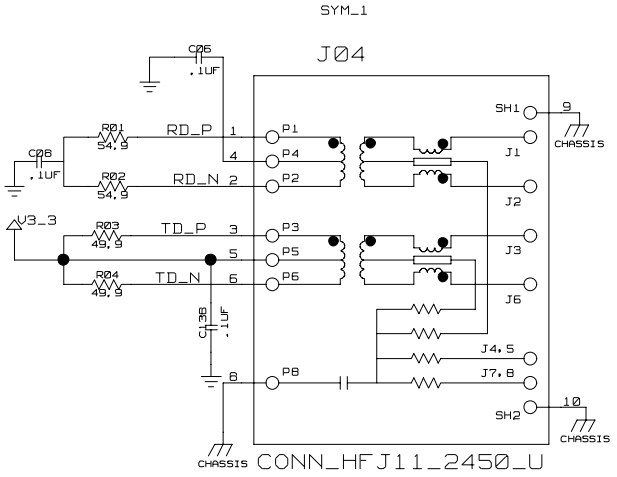


PLACEMENT NOTE:
TESTPOINTS (SHOWN ABOVE) MUST BE PLACED THE SAME FOR EACH PORT TO ALLOW USE OF A DIFFERENT PHY CARD IF DESIRED. PLACEMENT SHOULD ALLOW 0.2 BETWEEN CONNECTORS.

ON Z44 CARD ALL 4 PORTS MUST BE PLACED WITH EQUAL SPACING AND A COMMON CENTER LINE

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 11/71(TOTAL)





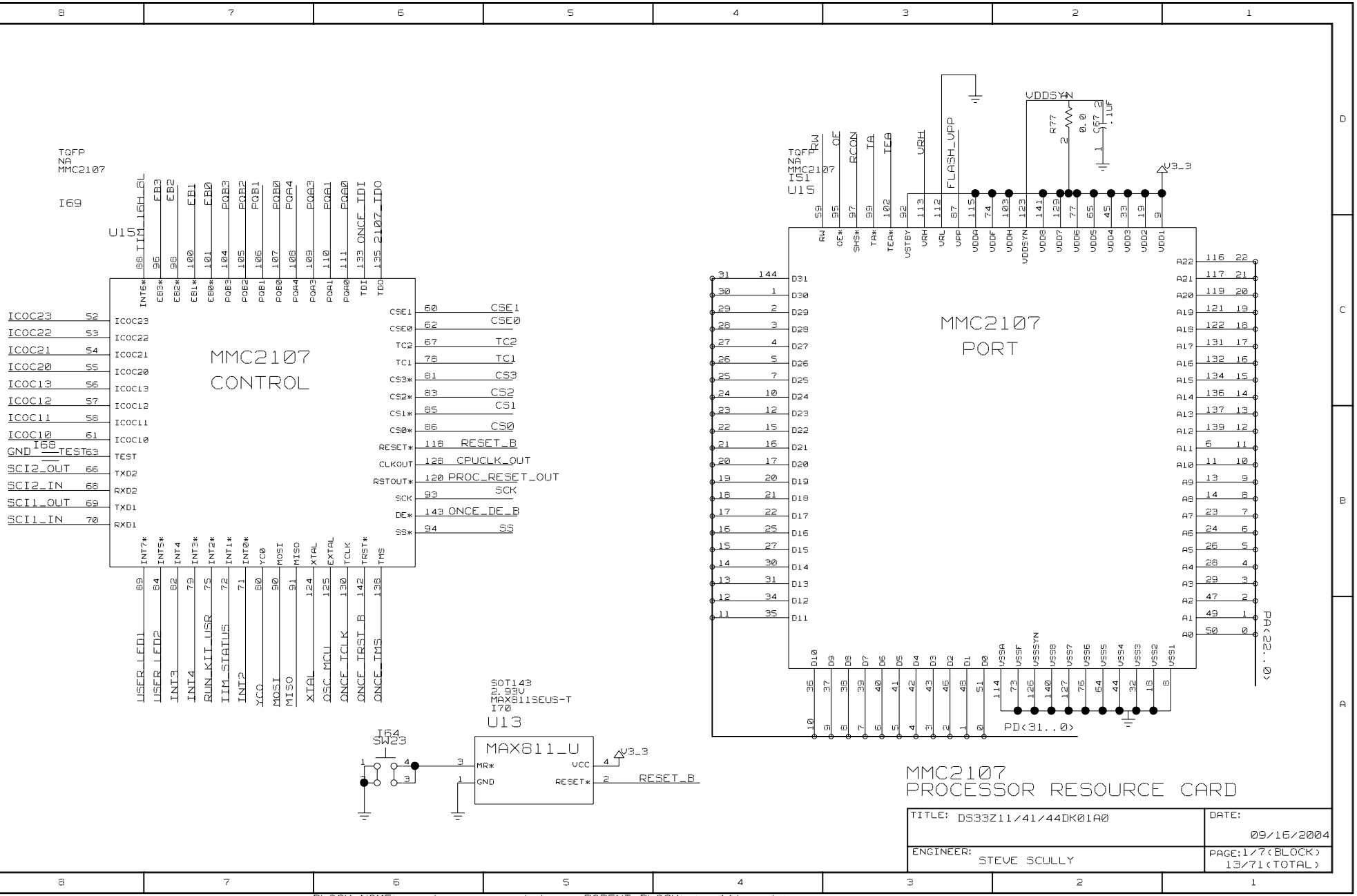
CAPS FOR XFRM CENTER TAP
SHOULD BE PLACED CLOSE TO XFRM

RESISTORS FOR TD+-/RD+-
SHOULD BE PLACED CLOSE TO PHY

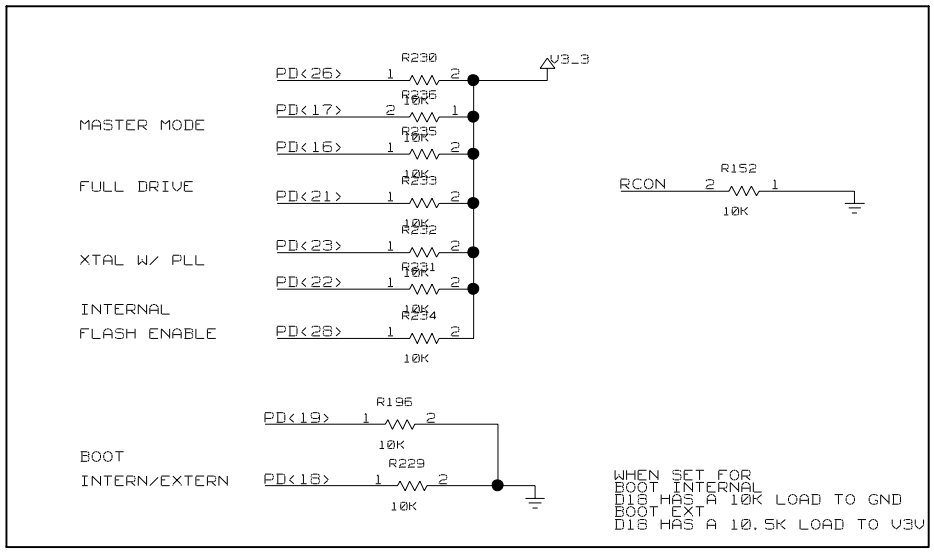
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:2/2(BLOCK) 12/71(TOTAL)

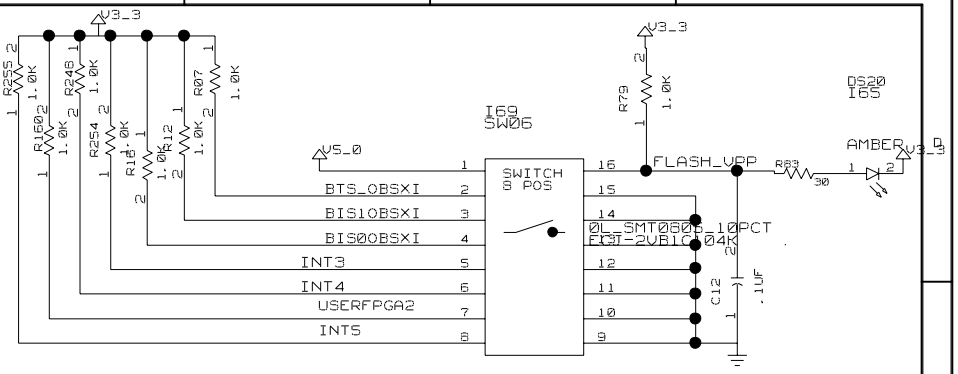
BLOCK NAME: _mii_wan_dn, PARENT BLOCK: _zllandlan_dn\

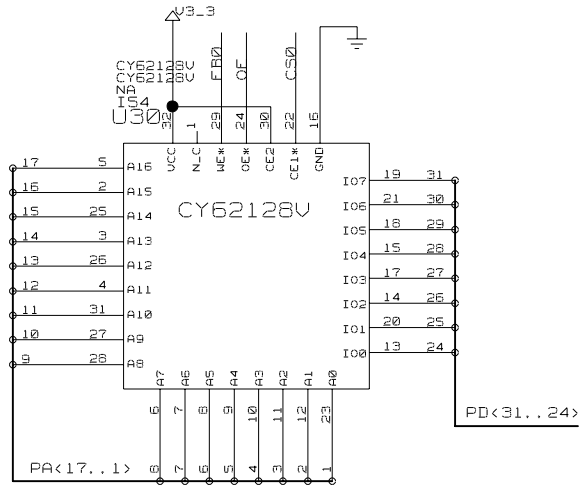
CR-13 : @_ztop_lib\,_ztopdn_\(sch_1):page1_15@_ztop_lib\,_zlltop_dn\(sch_1):page2_147@_ztop_lib\,_motprocrescard_dn\(sch_1):Page1

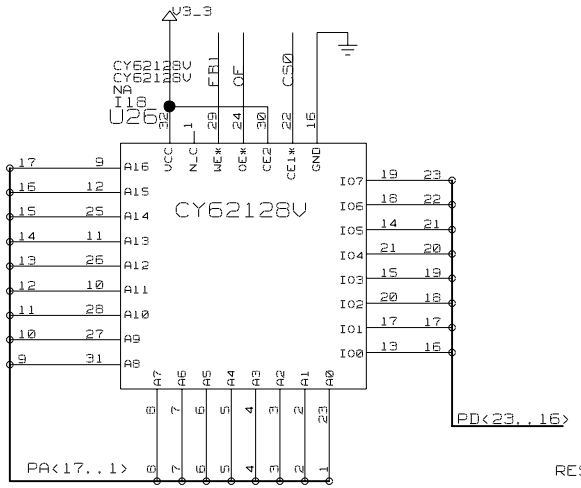


RESET CONFIGURATION





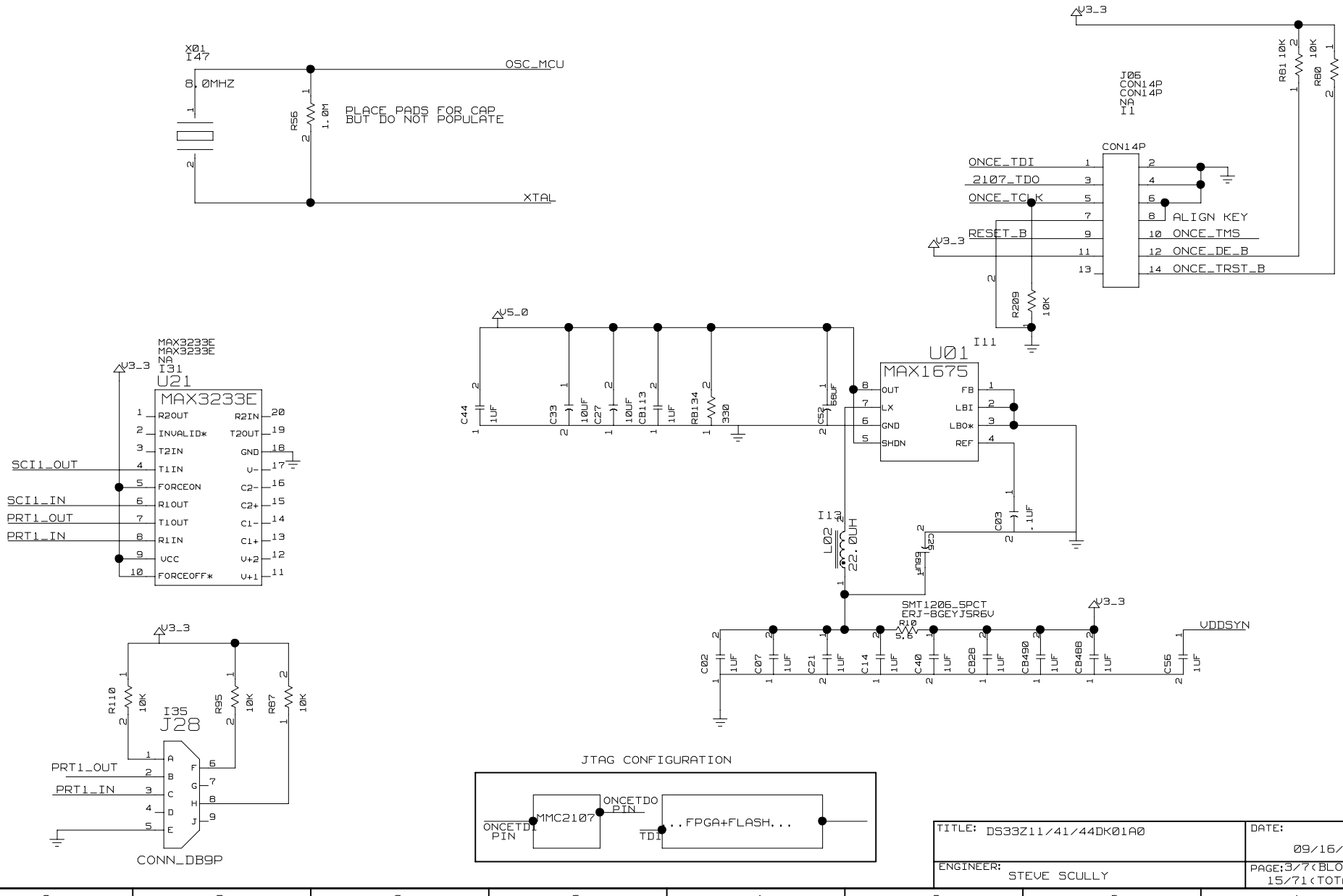




RESET AND CHIP CONFIGURATION

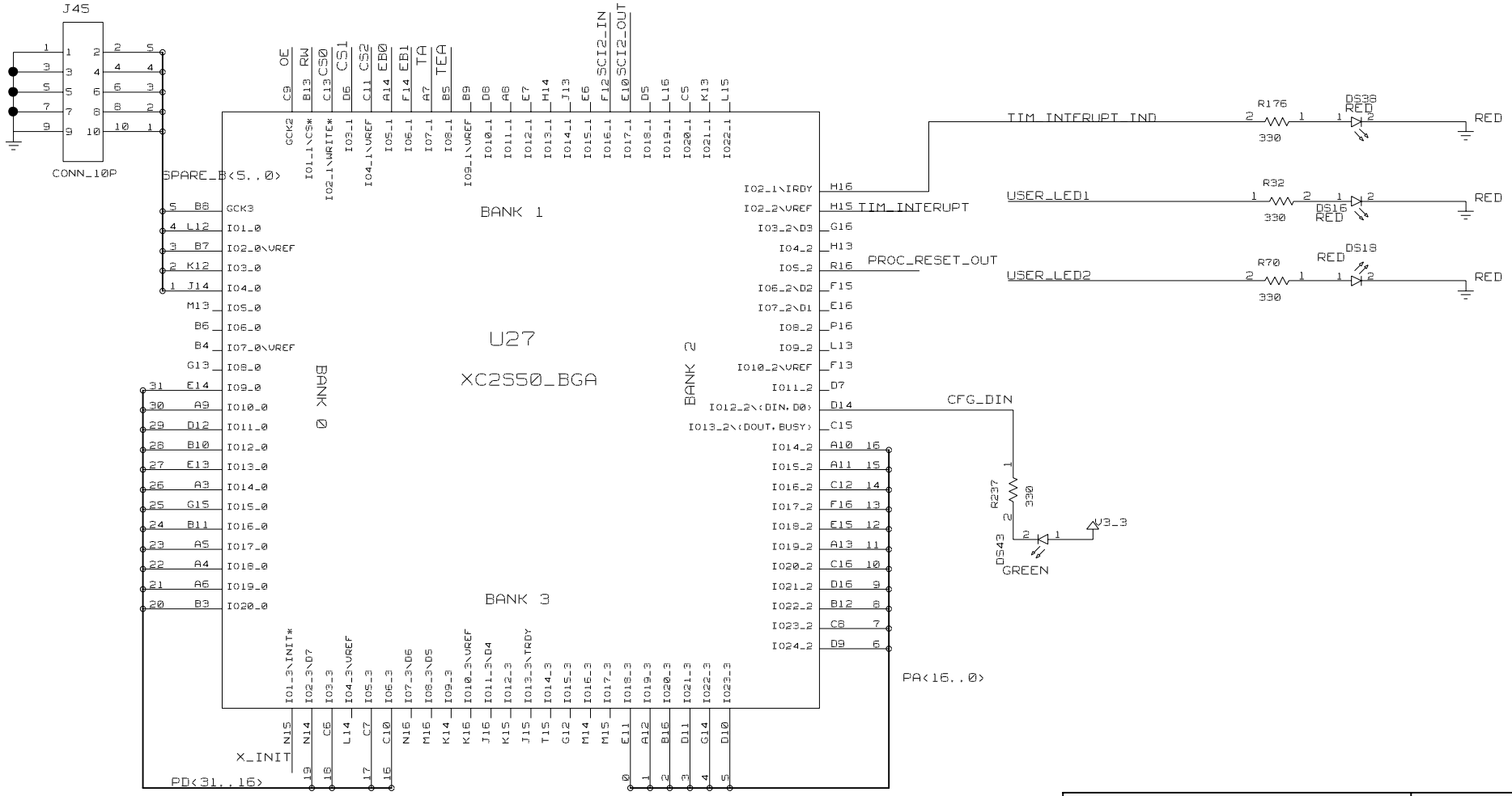
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:2/7(BLOCK) 14/71(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _zlltop_dn\



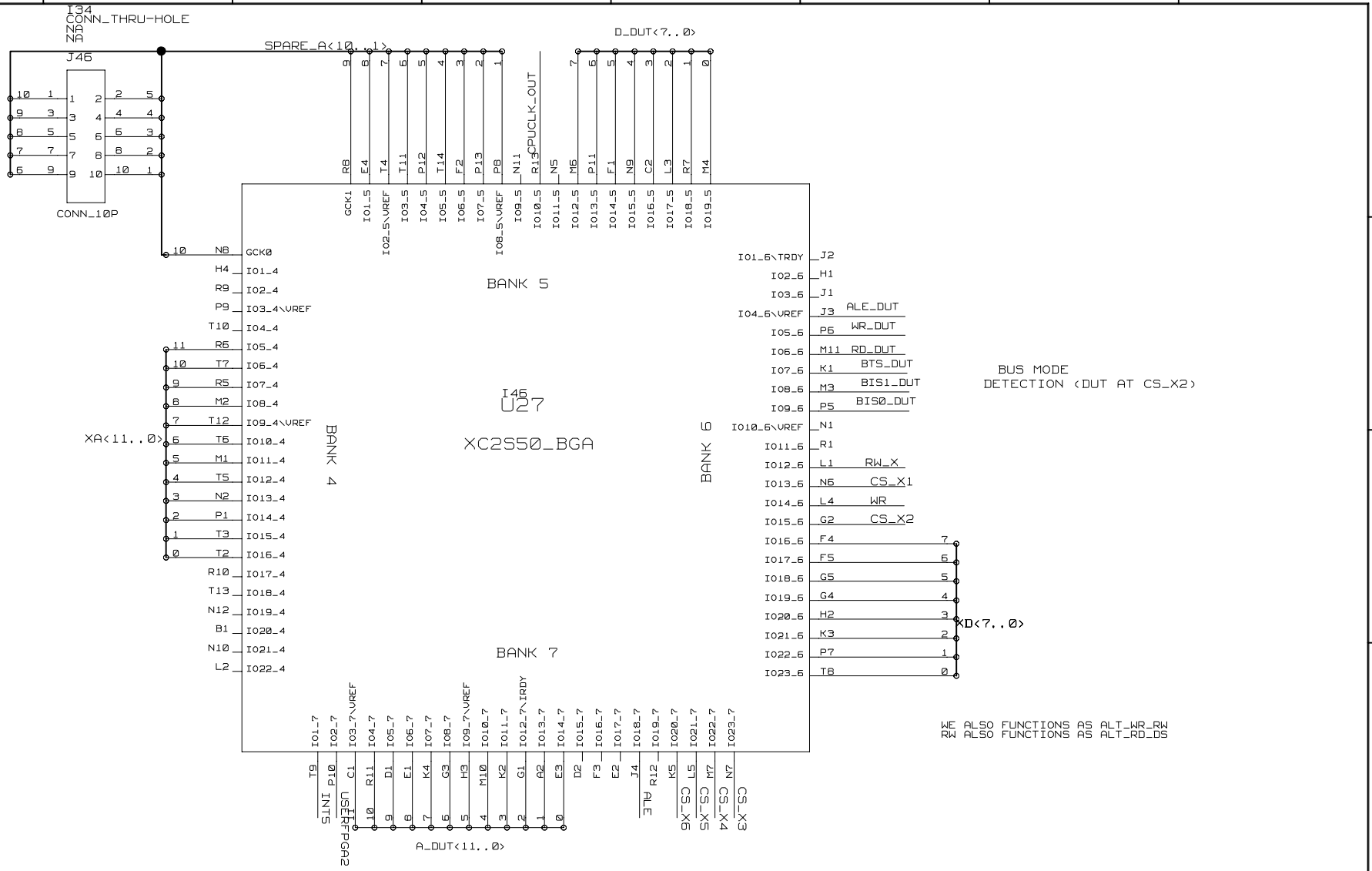
TITLE: DS33Z11/41/44DK01A0	DATE: 09/15/2004
ENGINEER: STEVE SCULLY	PAGE:3/7(BLOCK) 15/71(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _z11top_dn\



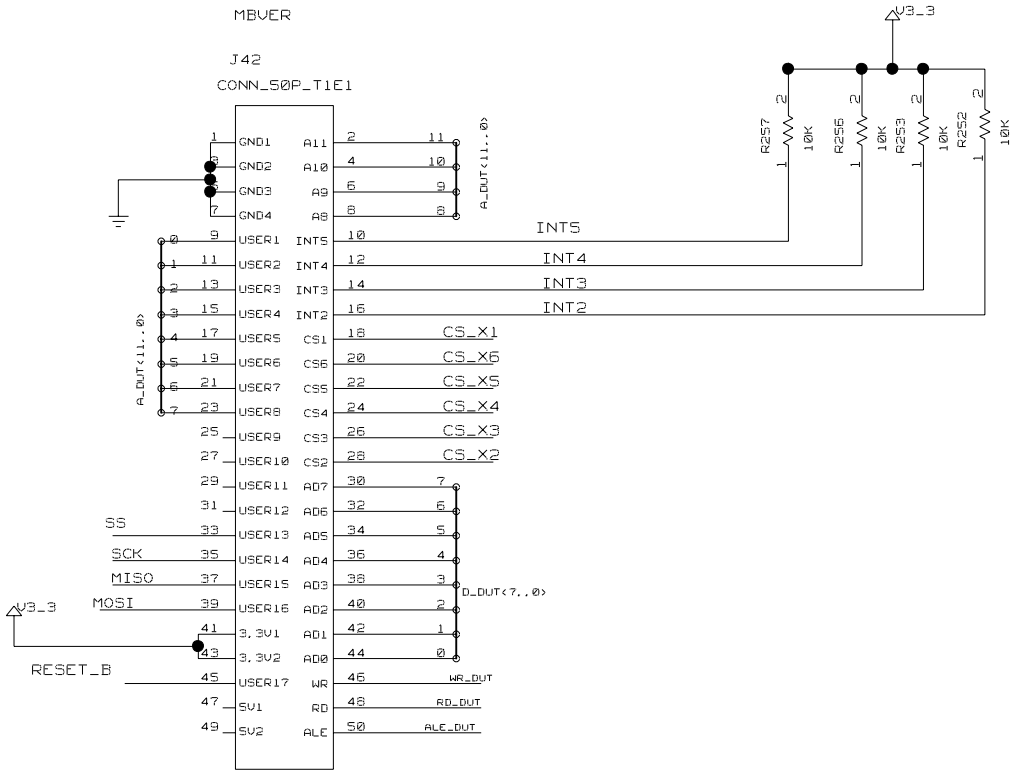
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:4/7(BLOCK) 16/71(TOTAL)

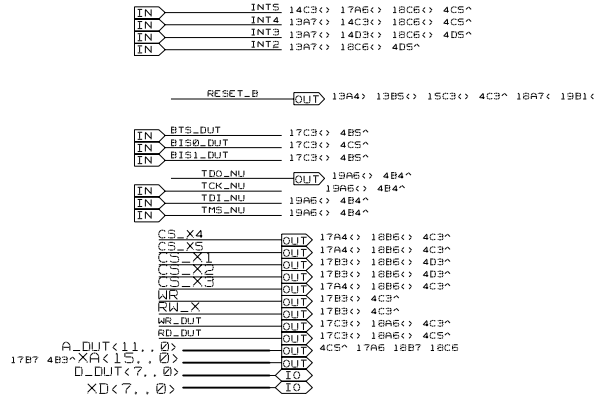
BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _zlltop_dn\



TITLE: DS33Z11/41/44DK01A0	DATE: 09/15/2004
ENGINEER: STEVE SCULLY	PAGE:5/7(BLOCK) 17/71(TOTAL)

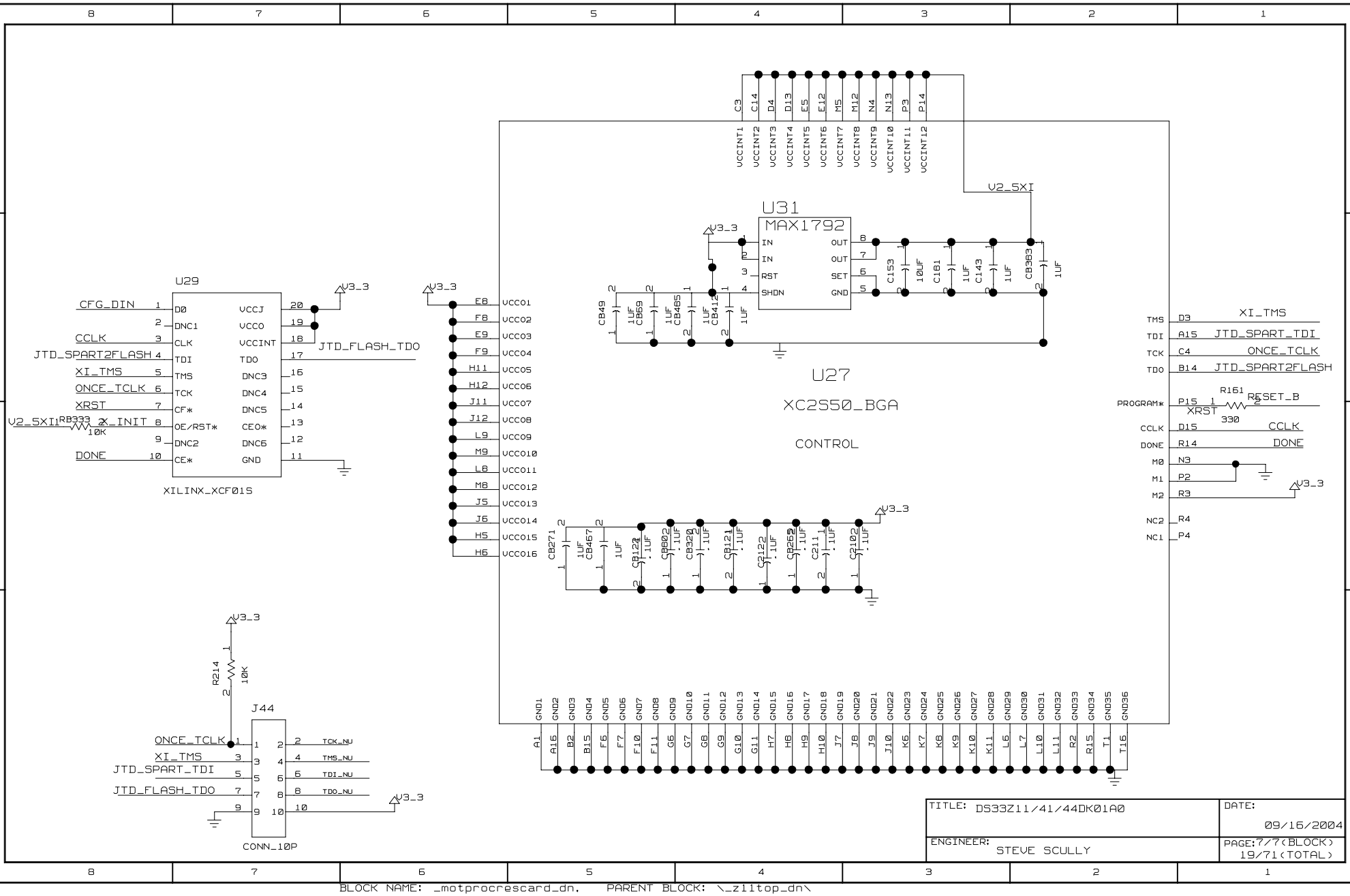
BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _z11top_dn\





TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:6/7(BLOCK) 18/71(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _zlltop_dn\



BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _z11top_dn\

DS21458 WAN INTERFACE BLOCK

I73
2.048MHZ_3.3V

YB02
OSC
V3_3
RB150 30 MCLK 46C7<
RB184 30 MCLK2FPGA 53B6<>

U20
DS21458_U
CONTROL

JTRST K14
JTMS J15 XI_TMS 52C1< 52C8<> 52A7<>
JTCLK J16 ONCE_TCK 52C1< 52C8<> 52A7<>
JTDI C10 JTD_FLASH_TDO 52C6<>
JTDO K13 JTD0458 52A7<>
INT* H5 WAN_INT 55D5> 46A4<> OUT
LIUC D9 LIUC 51D7<
MCLK1 H4 MCLK 46D7<
MCLK2 J12
RCLKI H9
RNEGI H10
RPOSI G8
TEST1 J14
TEST2 J13
TSTRST K15 RESET_AH 46A1<> IN
CS* M8 CS 55A4< IN
RD* A10 RD 55A2< 54C7<> IN
WR* C9 WR 55A3< 54C7<> IN

DVSS11 N4
DVSS12 N5
DVSS13 N6
DVSS21 D11
DVSS22 D12
DVSS23 D13

DVDD11 P4
DVDD12 P5
DVDD13 P6
DVDD21 C11
DVDD22 C12
DVDD23 C13
DVDD31 D3
DVDD32 E3
DVDD33 F3
DVDD41 L14
DVDD42 M14
DVDD43 N14
RVDD1 H1
RVDD2 J16
RVDD3 A9
RVDD4 T8
TVDD11 R6
TVDD12 T5
TVDD21 A11
TVDD22 B11
TVDD31 F1
TVDD32 F2
TVDD41 L15
TVDD42 L16

A<0> H2 0
A<1> E10 1
A<2> H3 2
A<3> G4 3
A<4> N7 4
A<5> B9 5
A<6> T7 6
A<7>/ALE_AS G2 7
A<8> H6 8
A<9> J11 9
ADDR<9..0> IN 54C7 55A5 55A7

AD<0> P8 0
AD<1> D10 1
AD<2> N8 2
AD<3> P7 3
AD<4> M7 4
AD<5> R7 5
AD<6> G1 6
AD<7> G3 7
DAT<7..0> IO 54C3 55A2 55A4

BTS B10 BTS 51C7<
MUX R8 MUX 51B7<
ESIBRD H8 ESIBRD 51C7<
ESIBS<0> J8 ESIBR0 51C7<
ESIBS<1> J9 ESIBR1 51C7<

DVSS31 D4
DVSS32 E4
DVSS33 F4
DVSS41 L13
DVSS42 M13
DVSS43 N13
RVSS11 N1
RVSS12 J1
RVSS13 M1
RVSS21 E16
RVSS22 H16
RVSS23 D16
RVSS31 A5
RVSS32 A8
RVSS33 A4
RVSS41 T12
RVSS42 T13
RVSS43 T9
TVSS11 R5
TVSS12 T5
TVSS21 A12
TVSS22 B12
TVSS31 E1
TVSS32 E2
TVSS41 M15
TVSS42 M16
NC1 K9
NC2 P3
NC3 E9

I37 NA NC7SZ86
I41 NA NC7SZ86
UX805 NC7SZ86_U INVERTER 52B1< 55D6<> RESET_B RESET_AH 46B7<

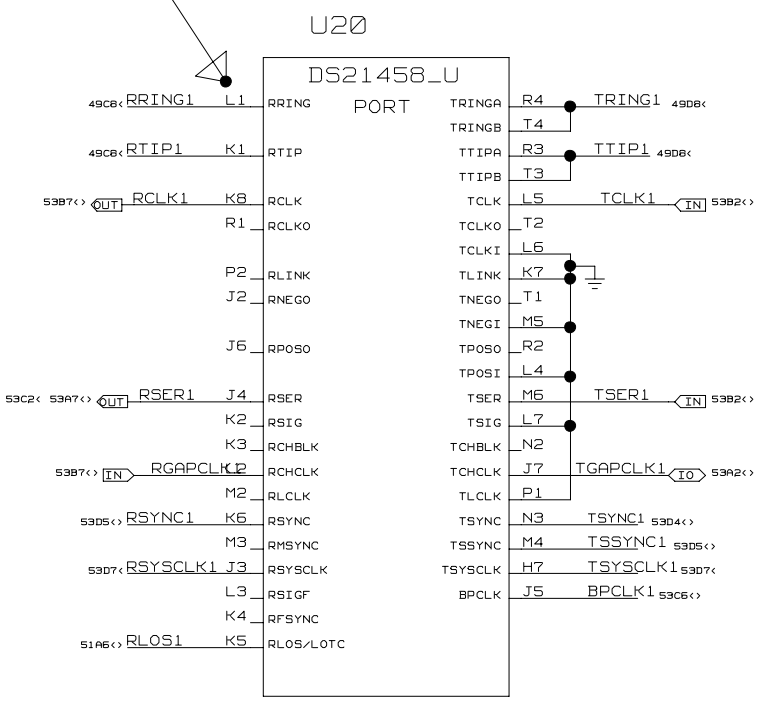
RED DS25 R114 330 V3_3 NC7SZ86_U BUFFER UX11 WAN_INT 46C7> 55D5>

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 46/71<TOTAL>

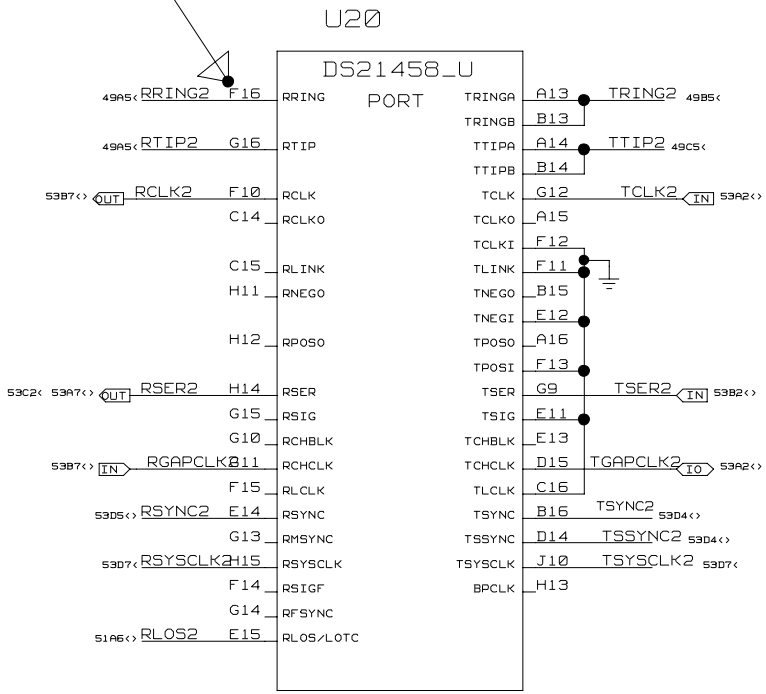
BLOCK NAME: _quadtelwan_dn, PARENT BLOCK: _wan4z44_dn\

PRINTED Tue Apr 26 14:22:56 2005

PORT1_RRING = PIN L1



PORT2_RRING = PIN F16



TITLE: DS33Z11/41/44DK01A0	DATE: 09/15/2004
ENGINEER: STEVE SCULLY	PAGE:2/10(BLOCK) 47/71(TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\

PORT3_RRING = PIN A6

U20

DS21458_U

PORT

50C8<	RRING3	A6	RRING	TRINGA	D1	TRING3	50D8<
				TRINGB	D2		
50C8<	RTIP3	A7	RTIP	TTIPA	C1	TTIP3	50D8<
				TTIPB	C2		
53B7<> OUT	RCLK3	G5	RCLK	TCLK	F6	TCLK3 IN	53A2<>
		A2	RCLKO	TCLKO	B2		
				TCLKI	F7		
		C3	RLINK	TLINK	G7		
		F8	RNEGO	TNEGO	A1		
				TNEGI	E5		
		F9	RPOSO	TPOSO	B1		
				TPOSI	D5		
53C2< 53A7<> OUT	RSER3	C8	RSER	TSER	G6	TSER3 IN	53B2<>
		B7	RSIG	TSIG	F5		
		C7	RCHBLK	TCHBLK	C5		
53B7<> IN	RGAPCLK3	D7	RCHCLK	TCHCLK	B4	TGAPCLK3 IO	53A2<>
		B6	RLCLK	TLCLK	C4		
53D4<>	RSYNC3	B5	RSYNC	TSYNC	B3	TSYNC3	53D4<>
		E6	RMSYNC	TSSYNC	A3	TSSYNC3	53D4<>
53D7<	RSYSCLK3	B8	RSYSCLK	TSYSCLK	D8	TSYSCLK3	53C7<
		E7	RSIGF	BPCLK	E8		
		C6	RFSYNC				
51A6<>	RLOS3	D6	RLOS/LOTC				

PORT4_RRING = PIN T11

U20

DS21458_U

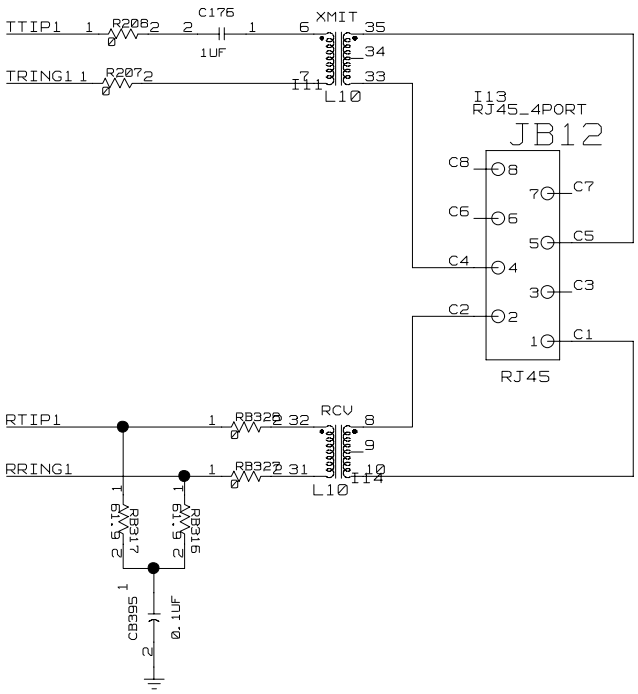
PORT

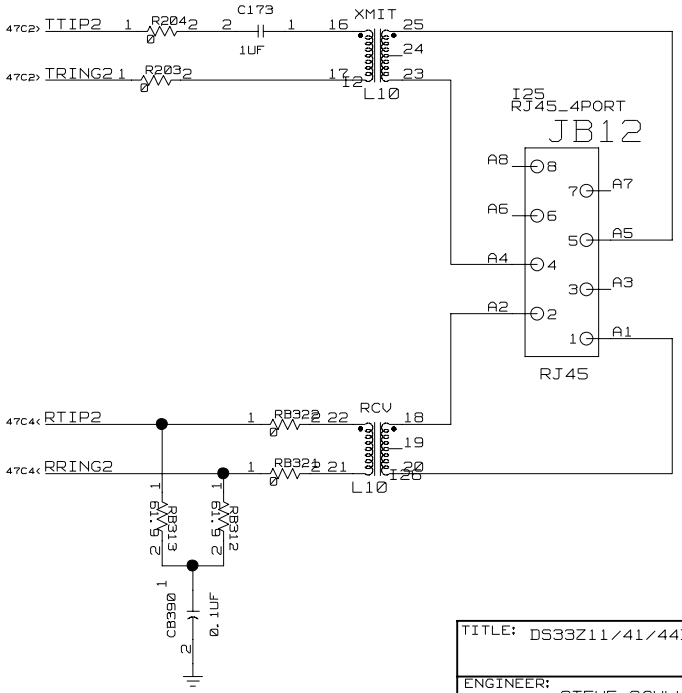
50A5<	RRING4	T11	RRING	TRINGA	N15	TRING4	50B5<
				TRINGB	N16		
50A5<	RTIP4	T10	RTIP	TTIPA	P15	TTIP4	50C5<
				TTIPB	P16		
53B7<> OUT	RCLK4	K12	RCLK	TCLK	L9	TCLK4 IN	53A2<>
		P14	RCLKO	TCLKO	R16		
				TCLKI	L11		
		T15	RLINK	TLINK	L12		
		P10	RNEGO	TNEGO	T16		
				TNEGI	M12		
		N10	RPOSO	TPOSO	R15		
				TPOSI	L10		
53C2< 53A7<> OUT	RSER4	P9	RSER	TSER	K10	TSER4 IN	53B2<>
		R10	RSIG	TSIG	K11		
		R11	RCHBLK	TCHBLK	R13		
53B7<> IN	RGAPCLK4	M9	RCHCLK	TCHCLK	P13	TGAPCLK4 IO	53A2<>
		R12	RLCLK	TLCLK	T14		
53D4<>	RSYNC4	N12	RSYNC	TSYNC	R14	TSYNC4	53D4<>
		M10	RMSYNC	TSSYNC	M11	TSSYNC4	53D4<>
53D7<	RSYSCLK4	R9	RSYSCLK	TSYSCLK	L8	TSYSCLK4	53C7<
		N11	RSIGF	BPCLK	N9		
		P11	RFSYNC				
51A6<>	RLOS4	P12	RLOS/LOTC				

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:3/10<BLOCK> 48/71<TOTAL>

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-49 : @_ZTOP_LIB\,_ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\,_WAN4Z44_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\,_QUADTE1WAN_DN\(SCH_1):PAGE4

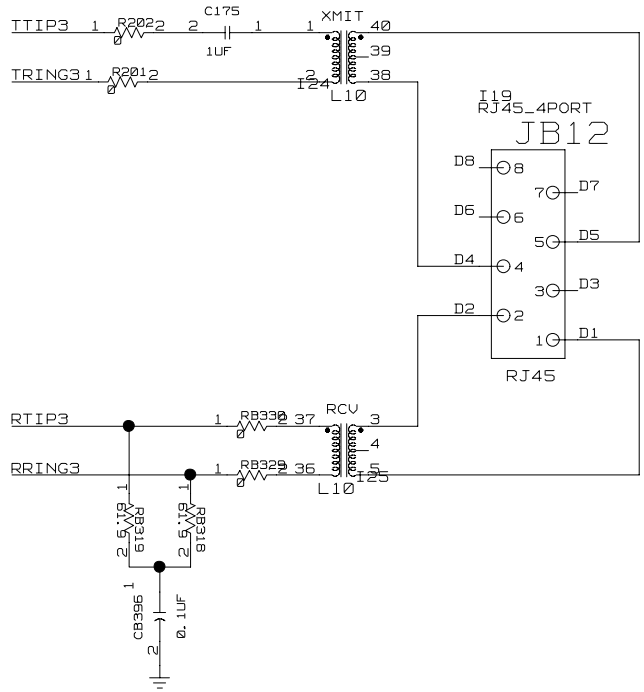


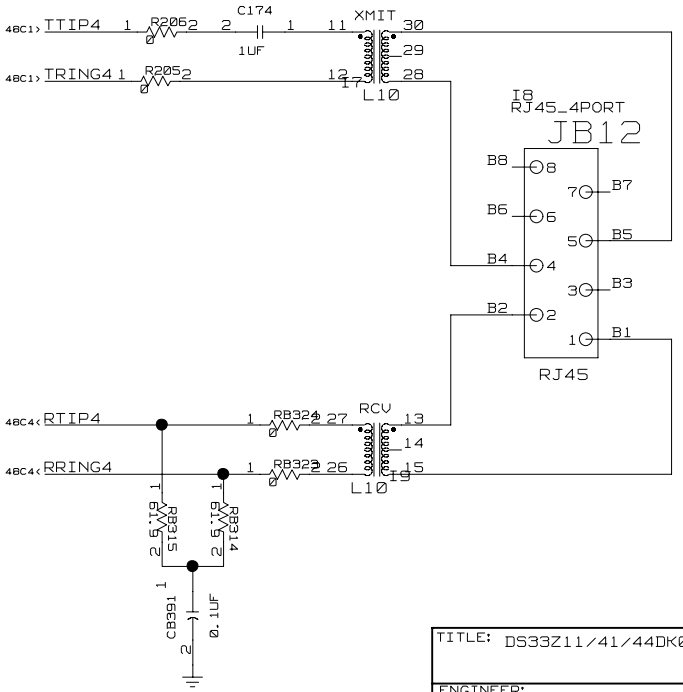


THE PCB LAYOUT INCORRECTLY USES PINS 38-40, 33-35, 28-30 AND 23-25
AS THE TX PRIMARY. THIS HAS BEEN CORRECTED IN THE SCHEMATIC,
THE PCB / ASSEMBLY HAS BEEN MODIFIED TO ACCOMMODATE THIS.

TITLE: DS33Z11/41/44DK01A0	DATE: 09/15/2004
ENGINEER: STEVE SCULLY	PAGE:4/10(BLOCK) 49/71(TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\

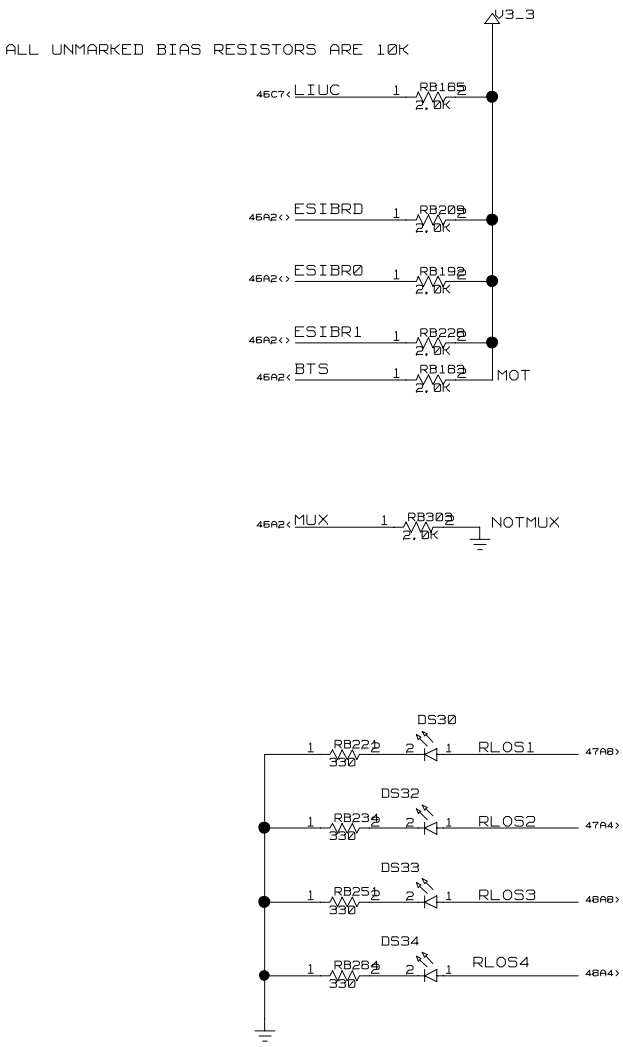




THE PCB LAYOUT INCORRECTLY USES PINS 38-40, 33-35, 28-30 AND 23-25 AS THE TX PRIMARY. THIS HAS BEEN CORRECTED IN THE SCHEMATIC, THE PCB / ASSEMBLY HAS BEEN MODIFIED TO ACCOMMODATE THIS.

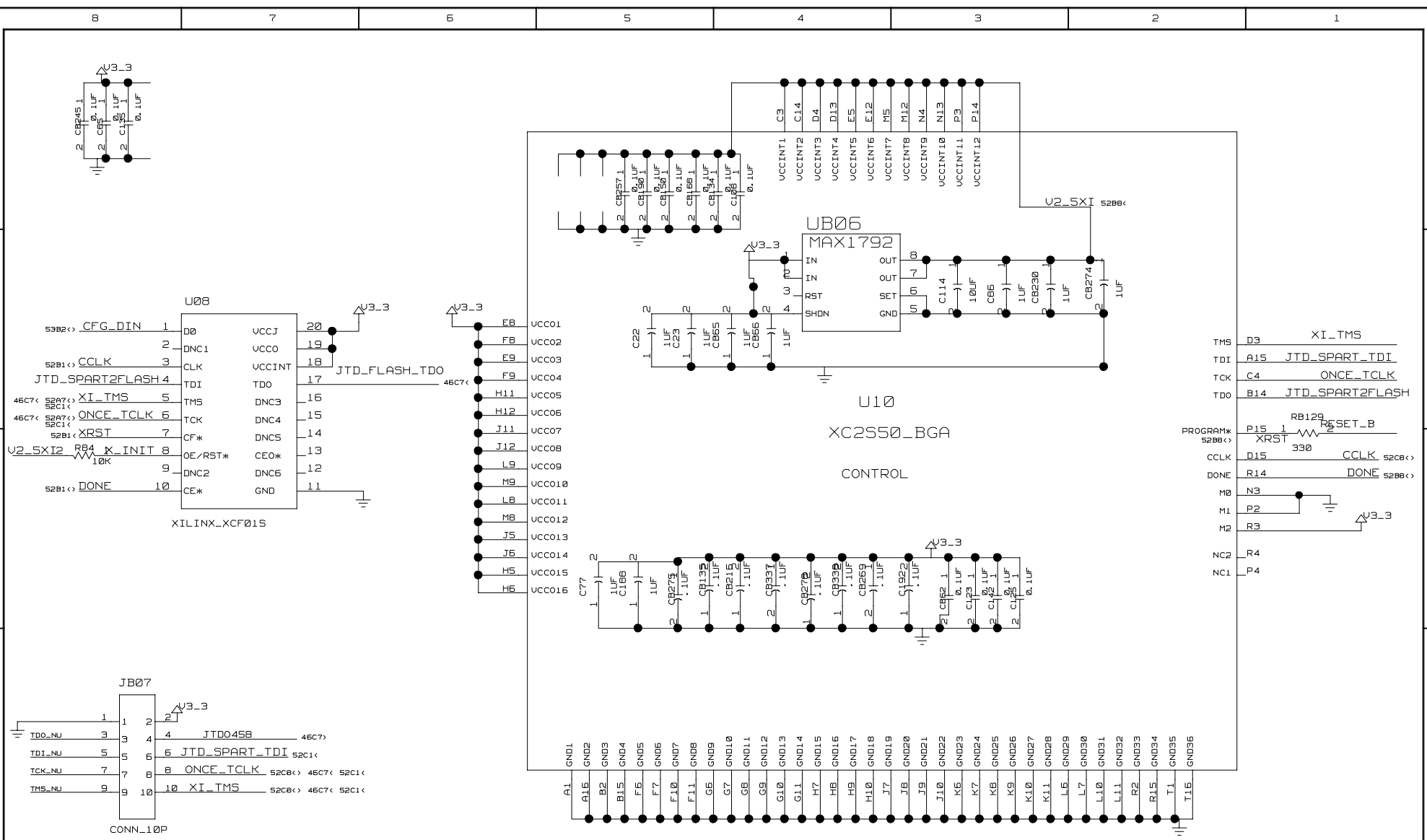
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:5/10(BLOCK) 50/71(TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\



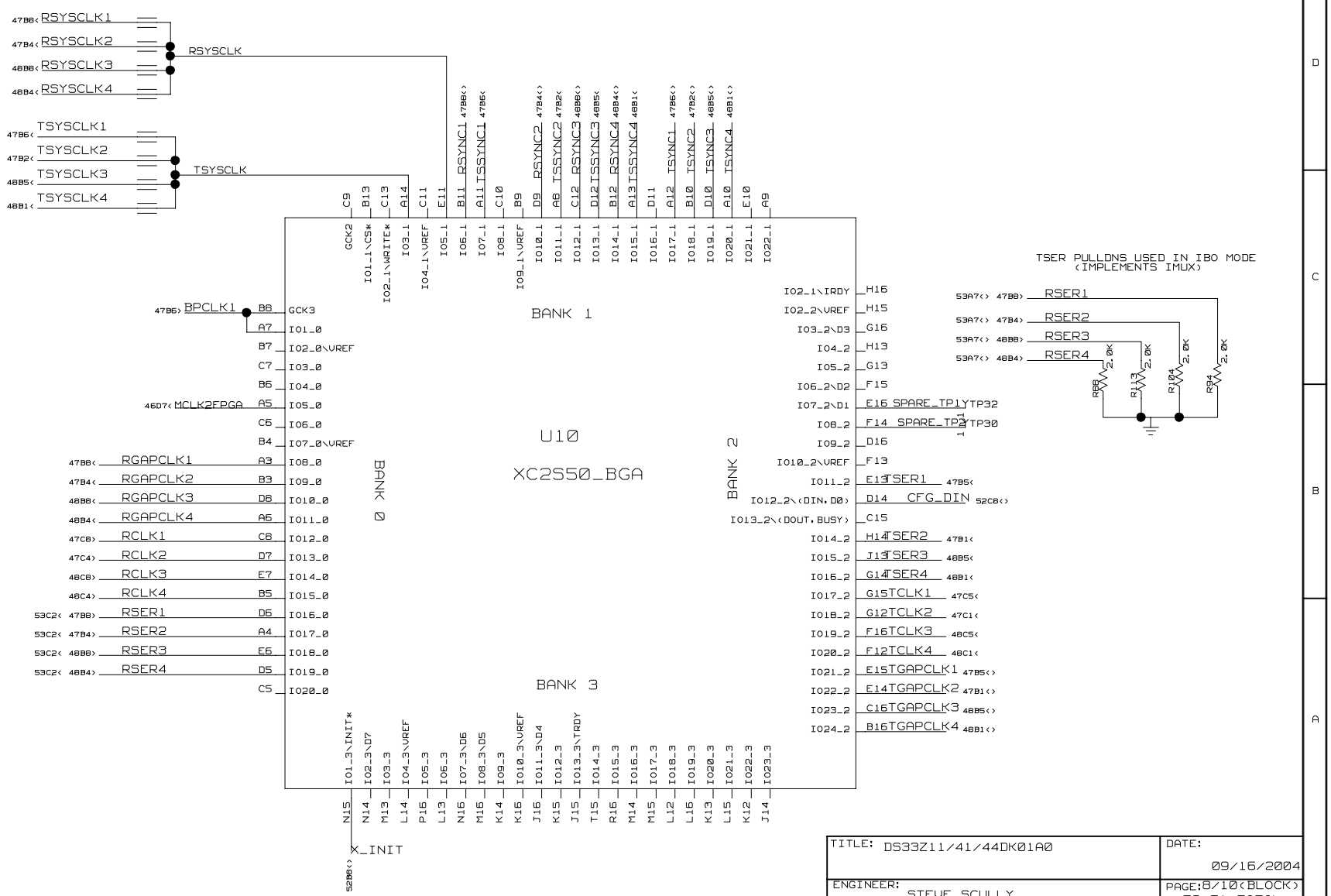
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:6/10(BLOCK) 51/71(TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\



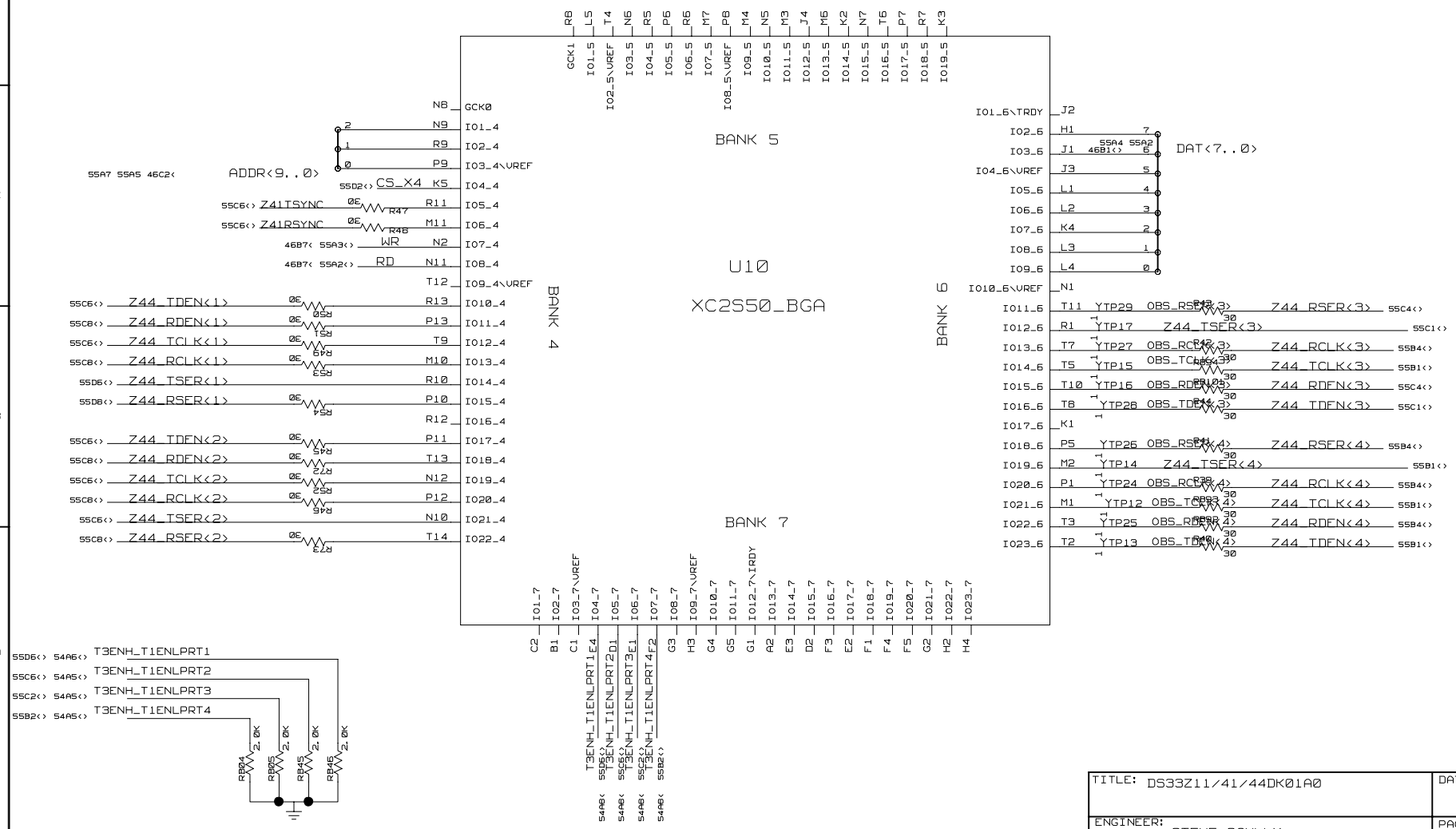
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:7/10(BLOCK) 52/71(TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:8/10(BLOCK) 53/71(TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\



TITLE: DS33Z11/41/44DK01A0	DATE: 09/15/2004
ENGINEER: STEVE SCULLY	PAGE:9/10<BLOCK> 54/71<TOTAL>

BLOCK NAME: _quadte1wan_dn, PARENT BLOCK: _wan4z44_dn\

V3_3
V3_3
GND

RECEPTACLE
P2 CONNECTOR (RECEPTICAL)

J12

VDD

	GND	71	1		
		72	2	I28 INT3	WAN_INT 46A4<> 46C7>
	INT5	73	3		
55D6<>	INT2	74	4	GND	
	GND	75	5	INT2 55D7<>	
		76	6	RESET_B 46A2<> 52B1<	
	GND	77	7		
	V3_3	78	8	T3ENH_T1ENLPRT1	54A6<> 54A8<
54B8<	Z44_RSER<1>	79	9	Z44_TSER<1>	54B8<>
	GND	80	10	GND	
	GND	81	11	SIG_RETURN	55A1> 55B2<> 55C6<>
54B8<	Z44_RDEN<1>	82	12	Z44_TDEN<1>	54B8<
		83	13		
	GND	84	14		
54B8<	Z44_RCLK<1>	85	15	Z44_TCLK<1>	54B8<
	GND	86	16	GND	
	GND	87	17	Z41RSYNC	54C7<
		88	18	Z41TSYNC	54C7<
		89	19	GND	
	V3_3	90	20	T3ENH_T1ENLPRT2	
		91	21		54A5<> 54A8<
		92	22	GND	
	GND	93	23	SIG_RETURN	55A1> 55B2<> 55C6<>
54A8<	Z44_RSER<2>	94	24	Z44_TSER<2>	54B8<>
		95	25		
	GND	96	26		
54B8<	Z44_RDEN<2>	97	27	Z44_TDEN<2>	54B8<
		98	28	GND	
	GND	99	29		
54B8<	Z44_RCLK<2>	100	30	Z44_TCLK<2>	54B8<
		101	31	GND	
	V3_3	102	32		
		103	33	GND	
	GND	104	34		
		105	35		
		106	36		
	GND	107	37		
		108	38		
		109	39	GND	
	GND	110	40		
		111	41		
		112	42		
	GND	113	43	GND	
	V3_3	114	44		
		115	45		
	GND	116	46	GND	
		117	47		
		118	48		
	GND	119	49		
		120	50		
		121	51		
	GND	122	52	GND	
52A8<>	TDI_NU	123	53	TDO_NU	52A8<>
52A8<>	TMS_NU	124	54	TCK_NU	52A8<>
	V3_3	125	55	GND	
		126	56		
		127	57		
	GND	128	58	GND	
		129	59		
		130	60		
	GND	131	61		
		132	62		
		133	63		
	GND	134	64	GND	
46C2< 54C7		135	65		
55A5		136	66		
	V3_3	137	67	GND	
	OSC2_NU	138	68		
	OSC4_NU	139	69	OSC3_NU	
		140	70	GND	

ADDR<9..0> — 0, 2, 4, 7, 9 — 55A5

ADDR<9..0> — 1, 3, 5, 6, 8

46C2< 54C7 55A7

55A2 54C3 46B1<>

P1 CONNECTOR (RECEPTICAL)
RECEPTACLE

J09

	GND	71	1		
		72	2		ALE
CS_X5		73	3		CS_X4 54C7<>
	GND	74	4	GND	
		75	5		
		76	6		
	GND	77	7	GND	
	V3_3	78	8		
		79	9		
	GND	80	10	GND	
		81	11		
		82	12		
	GND	83	13		
	GND	84	14		
		85	15		
		86	16	GND	
		87	17		
	GND	88	18		
		89	19	GND	
	V3_3	90	20		
		91	21		
		92	22	GND	
	GND	93	23		
		94	24		
		95	25	T3ENH_T1ENLPRT3	
	GND	96	26	Z44_TSER<3>	54A5<> 54A8< 54B1<>
54B1<	Z44_RSER<3>	97	27		
	GND	98	28	GND	
	GND	99	29		
54B1<	Z44_RDEN<3>	100	30	Z44_TDEN<3>	54B1<
		101	31	GND	
	V3_3	102	32		
54B1<	Z44_RCLK<3>	103	33	Z44_TCLK<3>	54B1<
		104	34	GND	
	GND	105	35		
		106	36		
		107	37		
	GND	108	38		
		109	39		
		110	40	GND	
	GND	111	41	T3ENH_T1ENLPRT4	
54B1<	Z44_RSER<4>	112	42	Z44_TSER<4>	54A5<> 54A8< 54B1<>
		113	43	GND	
	V3_3	114	44		
54B1<	Z44_RDEN<4>	115	45	Z44_TDEN<4>	54A1<
		116	46	GND	
	GND	117	47	SIG_RETURN	55A1> 55C6<>
54B1<	Z44_RCLK<4>	118	48	Z44_TCLK<4>	54B1<
		119	49		
	GND	120	50		
		121	51		
	GND	122	52	GND	
		123	53		
		124	54		
	GND	125	55	GND	
	V3_3	126	56		
		127	57		
	GND	128	58	GND	
	OSC1_NU	129	59		
		130	60		0
	GND	131	61		55A4
		132	62	54C3 46B1<>	1
		133	63		3
	GND	134	64	GND	
		135	65		5
		136	66		7
	GND	137	67	GND	
	V3_3	138	68		
		139	69	RD	54C7<> 46B7<
	WR	140	70	GND	

DAT<7..0> — 2, 4, 6 — I29 — CS — CS_X2 — CS_X3 — 46B7<

DAT<7..0>

NOTE 3184 IS ON CS3 WHILE 21455 IS ON CS2/CS4

GND — I27 — SIG_RETURN

WAN R.C. CONNECTOR TO MOTHERBOARD

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:10/10<BLOCK> 55/71<TOTAL>

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\